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Dear Dr. Nakane,

Enclosed is the final report "Characterization of Femtosecond Laser Machined Micro-wires". We would like to thank you for taking the time to review our work.

This project has the main objective of measuring the current-voltage relationship and relating the thermal property of the atom chip under the condition of high current. Several methods are suggested to carry out the testing process, and a detailed technical description of the testing apparatus is in the proposal. Introduction to some of the characterization devices are included.

Sincerely,

Anthony Siu
Bill Zhang

Characterization of Femtosecond Laser Machined Micro-wires

Anthony Siu

Bill Zhang

Project Sponsor:

Dr. Kirk Madison

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Executive Summary

Atom Chips are composed of micro-wires fabricated on a substrate. The wires are on a scale of micrometers: the thickness of the wires is $0.1\ \mu\text{m}$, the length of the wires is $4.8\ \text{mm}$, and the width of the wires range from 10 to $200\ \mu\text{m}$. For this project, the wires are straight with two large pads of $2\ \text{mm} \times 3\ \text{mm}$ at the end for contact purpose. They are designed to transmit high current through to generate magnetic fields for trapping cold atoms. At present, atom chips are commonly fabricated by the process of photolithography. However, this project is part of a research effort to investigate the efficacy of using Femtosecond (Fs) laser ablation for the Atom Chip fabrication process. This technique offers the advantages of reducing the number of processing steps necessary to create a prototype Atom Chip and eliminating the need for hazardous chemicals. The fabrication properties and characteristics are still unknown. Therefore, the purpose of this project is to develop a series of methods to characterize the current-voltage relationship of the chip. Furthermore, the thermal property of the chip is to be deduced from the I-V characteristics.

Atom chips fabricated with photolithography have been characterized of being capable of holding current densities of up to $10^7\ \text{A} / \text{cm}^2$. For this project, it is expected that the wire on the atom chip can hold a current of up to $5\ \text{A}$. After several iterations between chip prototyping and chip characterizing, the current capacity is expected to increase slowly as the project progresses. A testing apparatus is built for the project to test the electrical properties of the micro-wires on the chip. A constant current power source was used as an input, and the signals are observed on the oscilloscope. By analyzing the data from the signal, several time constants were determined on the electrical response of the system, and on the heating curve.

The project is intended to provide an idea of how much current atom chips created using Fs laser fabrication can support, and possibly come up with a mathematical model to predict how the temperature changes of the wire can affect the current sustainability. This result will become a guide for future chip designs. The testing apparatus is intended to make the characterization process easier and the documentation of the procedures on how to use the measurement devices will allow easier data replications.

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1.0 Background and Motivation

Atom Chips serve as a tool for the manipulation of cold atoms using carefully designed magnetic fields created by current-carrying micro-wires on planar chip structures. Atom Chips have been an active area of research in recent years. One aim is to apply Atom Chips to quantum information processing. Atom Chips have the potential to integrate storage, manipulation, and control of ultra-cold atoms and quantum degenerate gases. Atom chips are sub-mm micro-structures capable of having an extremely high current density on the orders of 10^7 A / cm^2 . [1] This allows the design of powerful magnetic fields above the planar chip surface which can allow the confinement of atoms with a magnetic dipole moment.

Currently, atom chips are fabricated by the traditional method of photolithography. This method uses a substrate (commonly Si, or sapphire) and gold as the conducting layer. In this work, Si is the substrate with a SiO_2 insulating layer that prevents current leakage out of the wires through the substrate. As an example, the microchip fabricated in the Heidelberg University in Germany has an area of $25 \times 30 \text{ mm}^2$. The thickness of the conducting layer is between 1 to $5 \text{ }\mu\text{m}$, and the width of the conducting wire can take values of 2, 5, 10, 50, and $100 \text{ }\mu\text{m}$. The thickness of the insulating layer is between 20 to 500 nm . According to their research, it was found that “wider wires heat up faster than narrow ones for equal current density”. [1]

Heat is a critical issue that determines the success or failure of a chip. If the chip heats up faster than it dissipates heat, the wire may fail, and damage the chip. Therefore, the design of the chip has to be oriented towards heat reduction. The substrate of the chip also acts as a heat sink that cools down the conducting wires. The conductance of the insulation layers has to be as high as possible to transfer heat from the wires to the substrate. The resistance of the wires is to be reduced in any possible ways to lower the power dissipation and thus the heat generated.

Other possible choices of the chip material have been used in the past. Sapphire has been successfully used for Atom Chip fabrication. However, Si has better surface, and adhesion qualities. In addition, Si can be manufactured with almost perfect surface smoothness.

1.1 Photolithography

Photolithography is the most popular modern technology for Integrated Circuit fabrications. It serves as the best combination of quality and economic values, making it a widely used process in both industry and lab environments.

Photolithography normally uses silicon as the substrate. A photo-mask is prepared with a circuit pattern etched with a laser. This photo-mask is then used to expose UV-light on the substrate that is coated with photo-resist. Then the photo-resist is processed in the etching solution and the pattern on the photo-mask is transferred onto the photo-resist.

Although the method of photolithography is common, it has its limitations. The resolution of photolithography is limited from 10 to 100 nm due to the diffraction of UV wave that travels through the photo-mask. The photo-mask is usually a transparent glass with the desired patterns on it. Since the glass has a different refractive index compared to air, the path of UV is slightly altered. This blurs the image on the edge of the patterns and creates resolution limit.

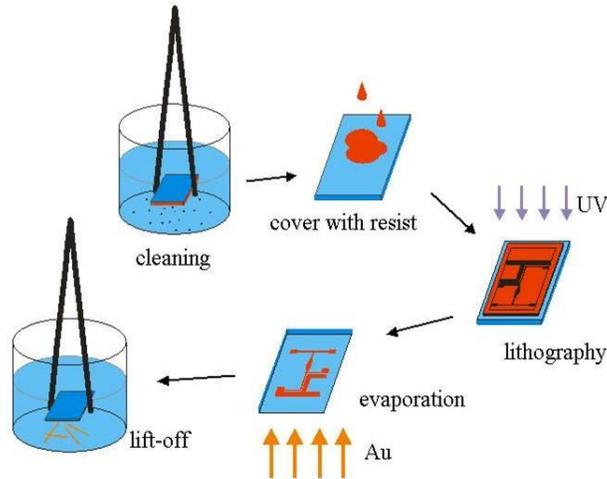


Figure 1.1: Lithographical Atom Chip Fabrication Process

<http://acqp.physi.uni-heidelberg.de/> [8]

1.2 Femtosecond Laser Ablation

With the continual diminishing size of electronic devices, traditional mechanical processes such as milling and drilling have reached a limitation in miniaturization. The Femtosecond (Fs, 10^{-15}) laser is an ultra-short pulsed laser. The Fs laser is known to be able to precisely ablate solid materials, with the accuracy and resolution capable of matching the laser's wavelength. [7] The article "Ablation and cutting of planar silicon devices using femtosecond laser pulses" from Laser Zentrum Hannover provides an overview of the principles of material ablation of Fs lasers.

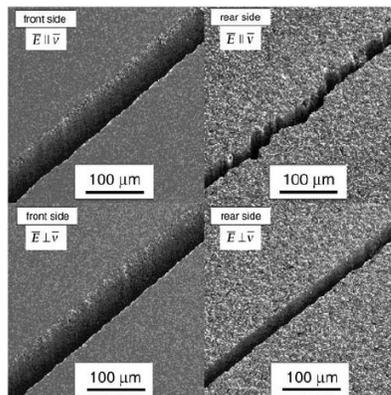


Figure 1.2: Femtosecond Laser cut of 100 μm thick Silicon [7]

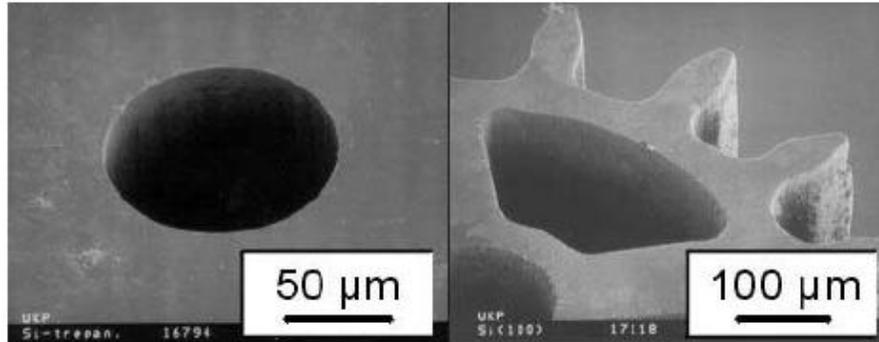


Figure 1.3: Silicon Structuring with Fs laser [7]

The primary application of the Fs laser in this project is to ablate the surface conducting material of the atom chip in order to build circuits. This is an innovative approach over traditional Lithography and surface morphological characterization is required. A goal of the project is to test the limits of the ablation abilities of the Fs laser available in the Chem. / Physics Building of UBC. The above Figure 1.2 shows the front and rear sides of a silicon ablated with the Fs laser at different polarization. The lower Figure 1.3 shows some of the possibilities of Fs laser structuring on silicon.

The Femtosecond (Fs) laser is able to ablate materials accurately and efficiently. Atom Chips have seen great success with standard lithography capable of high current densities of greater than 10^7 A/cm^2 , voltages of greater than 300 V, and fabrication resolution of less than $1\mu\text{m}$. [8] However, the Fs technique offers the advantages of reducing the number of processing steps necessary to create a prototype Atom Chip and eliminating the need for hazardous chemicals. The whole Fs laser technique is comparable to the first step in lithography, but directly cutting the conducting layer on the substrate rather than passively cutting the photo-mask and then transferring the photo-mask pattern on the photo-resist on the substrate.

By combining the merits of the Atom Chip with the state-of-the-art microfabrication process of Fs laser ablation, the project's aim is to create a well characterized Atom Chip. The main motivation of this project is the eventual patterning of the Atom Chip using the Fs laser such that a Magnetic Quadruple Trap can be formed close to the surface of the Atom Chip. The high current density requirement for the atom trap is unmanageable for regular PCBs. Although, the actual construction of the atom trap is beyond the scope of this project, this project will lay the foundation and provide the necessary technical preparations of Atom Chip microfabrication using Fs laser.

1.3 Motivation: Atom Chip as an Atom Trap

For experimental purposes, it is necessary to confine the atoms within a small volume. This can be achieved by cooling the atoms and then using a magnetic quadruple field to trap the atoms. The U-trap and Z-trap wire configurations and magnetic fields are illustrated in figure

1.4. The micro-wires require a current of up to 5 A to create a field large enough to confine the atoms.

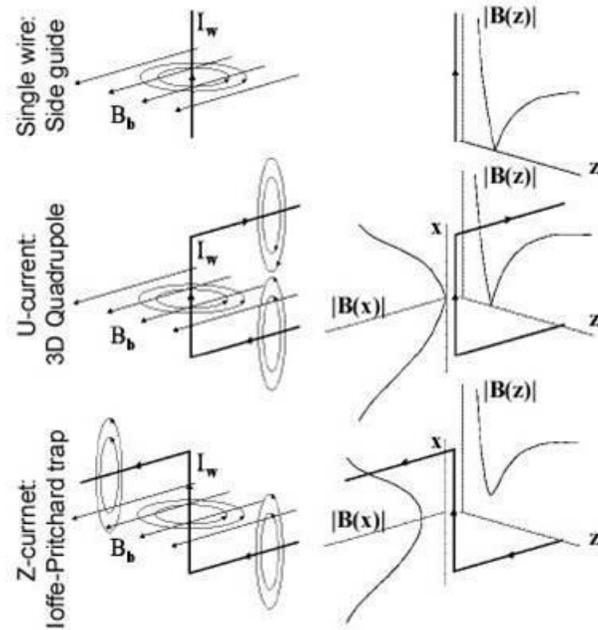


Figure 1.4: Magnetic Trapping Potential

<http://acqp.physi.uni-heidelberg.de/> [8]

2.0 Discussion

The Project objective is to characterize a set three experimental atom-chips that were manufactured by the project sponsor. By providing detailed documentations on the methods and testing protocols, this report is intended to provide the necessary technical background for those carrying forth this project. This project is still in the experimental stage where the prototype chips are characterized. By discussing the results of the characterizations, this report can assist in the design of future chips.

2.1 Project Objectives

The project portions involving the characterizations of the chips will be the responsibility of the APSC 479 student group, while the chip prototyping work (including Fs laser instrumentations) relies on Dr. Kirk W. Madison's research group of the Quantum Degenerate Gases (QDG) Lab; mainly Dr. James Booth and Dr. Bruce G. Klappauf. The following is a list of the sub-objectives:

The surface patterns should be characterized by the White Light Interferometer, the Scanning Electron Microscope, and the Profilometer. The dimensions of the wire are to be measured and cross-compared to determine the desired width. Any additional surface information picked up during the characterization process is helpful to guide the fabrication process.

Since the gold layer is non-adhesive to the solders, a special device should be constructed to connect the wire with other devices. The devices include constant current source, oscilloscope, function generators, and multimeters. The measurement should reveal the heating characteristic of the wires as well as their time constants. The data will be analyzed in Matlab.

The technique for characterizing the current-carrying capacity of the micro-wires must be devised. A routine procedure should be designed to measure the current-voltage relationship and the thermal properties of the micro-wire. This procedure should include a simple and reproducible mounting and removal method for the Atom Chips in the testing apparatus.

The testing of the I-V characteristics will require a pulsed current power supply rather than a constant current source. According to the research paper [1], the safety limit of a current pulse is around $1 \mu\text{s}$. For the testing in this project, current pulses of up to 500 ms long have been used and even constant currents have been used.

All the measurement procedures involving the use of the White Light Interferometer, the SEM, the Profilometer and the testing bench are to be clearly documented in detail for the groups that will continue this project. Also, testing protocols on the I-V characteristics should also be described and recorded so that the next group can repeat the measurement.

2.2 Technical Background

This section will describe some of the technical background pertaining to the three prototype atom chips that were manufactured by the sponsor. Information on the material of the chip, the general dimensions, and some notes during manufacturing are included. Some basic calculations based on the material properties of the chip will also be performed. In addition, the technicalities of the contact connection with the wire pads of the chips will be discussed.

2.2.1 Prototype Chip Details

The three prototype chips will be referred to as chips 1, 2, and 3 in this report. Some manufacturing note provided by the sponsor is that the chips are placed on a computer controlled stage and are moved under a stationary Femtosecond laser to ablate the surface pattern. Some of the ablation was carried out with higher power output from the laser while other cuts were made with a lower power output but ablated back and forth several times.

The three prototype atom chips that were manufactured are half inch square in area and are 0.15" thick. There are three main layers on the chips. The substrate used was SiO_2 covered by a thin adhesion layer of chromium followed by a conducting 0.1 μm thick layer of gold. The gold is covered with an unknown thickness of protective magnesium fluoride.

There are three straight wires ablated on the chip using a Femtosecond laser and there are pads on both sides for making the external connections. Figure 2.1 shows an overview photo of the chip and Figure 2.2 below shows the wire pattern on the surface of the chip. The length of the wires are 4.8 mm and the intended width of the three wires in the figure are arranged from left to right 200 μm , 100 μm , and 50 μm .

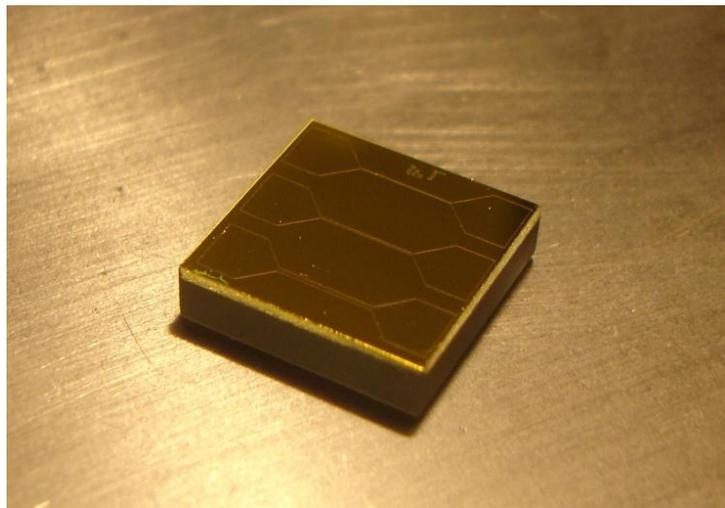


Figure 2.1: Overview of the Chip – half inch square in area

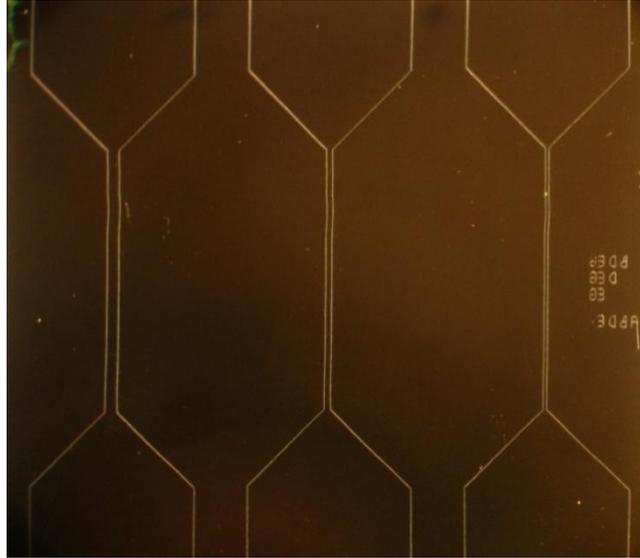


Figure 2.2: Chip Surface Wire Pattern

For this report, the collected data and analysis are on the individual wires on the chip. Due to time constraints, not all the wires on every chip were tested with all the testing protocols. The analysis will refer to the specific wires by the chip number (1 – 3) and the intended width for the wire. The intended width is the width which was desired / programmed during the manufacturing process of the chip. Unless specified, any reference to width in this report is the intended width.

Some chip specific information is listed here. Chip 1 is considered the bad chip because that is first prototype chip that was manufactured. The sponsor has mentioned that one of the micro-wires on chip 1 is a double wire because he was unsure whether the wire is cut, so that the particular wire was ablated again using a lower energy output from the laser. Chip 2 and chip 3 are considered the good wires, but one wire on chip 3 is also ablated twice.

The intended widths in μm for the three chips are listed here.

Chip 1	50	20	10
Chip 2	200	100	50
Chip 3	50	20	10

Table 1: Micro-wires Intended / Programmed Widths

2.2.2 Resistance Calculations based on Gold Properties

Since the micro-wires on the atom chips are composed of gold, some preliminary calculations can be performed to calculate the resistance values of the wires. Another calculation is to calculate what resistance the micro-wires will become when the wire is heated to 100°C . The sponsor has mentioned that the electrical IV testing should stay below 100°C .

Property	Value
Resistivity (ρ)	$2.44 \times 10^{-8} \Omega \text{ m}$

Linear coefficient of resistivity (α)	0.0034
Mass density of gold	$19.3 \times 10^3 \text{ kg/m}^3$
Specific heat capacity of gold	0.1291 kJ/kg K

Table 2: Properties of Gold

$$R = \frac{l \times \rho}{A}$$

Equation 1: Wire Electrical Resistance

$$R(T) = R(T_0)(1 + \alpha\Delta T)$$

Equation 2: Linear Electrical Resistance change with Temperature Change

Resistance₂₀ = Resistivity (Length) / Area

Resistance₁₀₀ = Resistance₂₀ (1+ Linear Resistivity Coefficient (100°C – 20°C))

Mass = Density (Area) (Length)

Area = (Width) (Wire Thickness = $0.1 \times 10^{-6} \text{ m}$)

Length = $4.8 \times 10^{-3} \text{ m}$

Wire Width (μm)	R ₂₀ (20°C) [Ω]	R ₁₀₀ (100°C) [Ω]	Wire Mass (kg)
10	117.12	148.98	9.26E-11
20	58.56	74.49	1.85E-10
50	23.42	29.80	4.63E-10
100	11.71	14.90	9.26E-10
200	5.86	7.45	1.85E-09

Table 3: Resistance of the Micro-wires based on Gold Properties

2.2.3 Four Point Contact Measurement

The contact between the measuring device and the wire of the chip is suspected to possess a large resistance. Connection pads were designed on the chip for making the electrical connection between the wire and external electrical instruments. When measuring the voltage, it would appear as if the contact resistance and the wire resistance are connected in series, thus the measured current will be lower than the actual current. To fix this problem, a contact trick called four point contact measurement is adopted into the design.

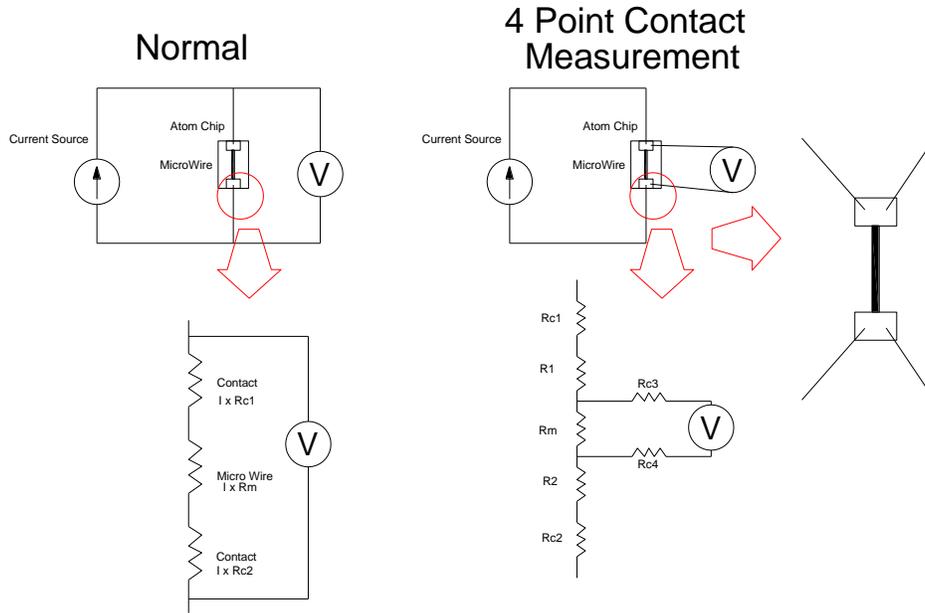


Figure 2.3: Four Point Contact Measurements

In order to determine the resistance of the Atom Chip wire, a current is applied through the micro-wire and the voltage is measured. The resistance of the micro-wire is denoted by R_m in the figure, and it is the resistance of interest. In the normal measurement case, the two contact leads which also have their own resistances, denoted by R_{c1} and R_{c2} , are also incorporated within the measurement. These values will affect the measured resistance of the micro-wire. In the case of the 4 point Contact measurement, the contact resistance R_{c3} and R_{c4} and R_1 and R_2 are introduced. R_1 and R_2 are the resistance of the area pad, and they should be small due to resistance being inversely proportional to area. R_3 and R_4 are the contact resistance from the leads of the voltage measurement device. However, now the voltage drop across R_{c3} and R_{c4} are relatively little because of the high impedance of the measuring device and the connection is parallel rather than in series (very low current across R_{c3} and R_{c4}). The voltage measured from this case is mostly contributed by the voltage drop from the resistance of the micro-wire.

2.3 Theory

In the fabrication and characterization processes of the atom chips, the key theories are: Heat Transfer, and Fs Laser Ablation.

2.3.1 Atom Chip Heat Transfer Theory

As mentioned, heat dissipation is the major factor that decides the success or failure of the micro-fabricated atom chip. If too much heat is generated by the wire in a short period of time, the heat may not be dissipated quickly enough and cause damage to the wires. Therefore, careful analysis of heat dissipation is crucial to the project. The only source of heat generation is by the power consumption of the conducting wire due to its own resistance. The power consumption is calculated by the equation below.

$$P = I^2 \cdot R = \frac{V^2}{R} \qquad R = \frac{L}{A} \cdot \rho = \frac{L}{A} \cdot \rho_0(\alpha(T - T_0) + 1)$$

Equation 3: General Power Consumption

Resistance (R) is a function of temperature (T) and power (P) is a function of R. In the equation above, “I” represents the current, and “P” is the power dissipation in the form of heat. As the temperature increases, the resistance of the wire also increases. Therefore, the power dissipation is not a constant value but a function of time. The generated heat is the integral of the power with respect to time.

The heat transfer can be separated into two steps: heat transfer from the conducting layer to the substrate through the insulating layer, and the temperature increase of the substrate due to heat transfer. The first process happens almost instantaneously at around 1 μ s. This time scale is give by the equation below:

$$\tau_{\text{fast}} = C_w h / (k - h j^2 \alpha \rho)$$

Equation 4: Time Constant of Heat Flow from Wire to Substrate through Insulator [1]

C_w is the heat capacity of the wire, h is the height of the wire, k is the thermal conductance of the substrate through the insulation layer, j is the current density, α is the linear scaling factor of the resistivity, and ρ is the resistivity. The following equation estimates the temperature difference between the conducting layer and the substrate. If the temperature difference is too large, the excess heat will damage the chip even before it can be transferred to the substrate.

$$\Delta T_f(t) = \frac{h \rho j^2}{k - h j^2 \alpha \rho} (1 - e^{-t/\tau_{\text{fast}}})$$

Equation 5: Temperature Difference between Wire and Substrate [1]

The temperature rise of the substrate is calculated by the equation below:

$$\Delta T_s(t) = \frac{h w \rho j^2}{2 \pi \lambda} \Gamma\left(0, \frac{C_w^2}{4 \pi^2 \lambda t}\right) \approx \frac{\rho I j}{2 \pi \lambda} \ln\left(\frac{4 \pi^2 \lambda t}{C_w^2}\right)$$

Equation 6: Temperature Change of Substrate [1]

The new variable λ is the heat conductivity. In this process, heat is transferred to the substrate due to the temperature difference built up in the previous step. In the equation, one can see that the temperature rise of the substrate is non-linear-inversely proportional with the width of the wire. This means, if the wire is wider the temperature rise of the substrate is lower. Therefore, less heat is absorbed by the substrate and the temperature of the wire is higher. Mean while, if the wire is narrower, the temperature of the substrate will increase more. As a result, more heat is absorbed by the substrate and the temperature of the wire is lower.

From the equations, one can see that there is a tradeoff on the width of the wire and heat dissipation. If the wire is wider, the resistance of the wire is lower and less heat is generated. However, the heat transfer is also slower which means that it is harder to cool down.

On the other hand, if the wire is narrower, the resistance of the wire is higher and more heat is generated. However, the heat is transferred faster to the substrate. The experimental data from this project can help finding the optimum wire dimensions. The temperature data may be fitted against the equations shown within this section.

2.3.2 Time constant of Wire

Similar to capacitors, resistors have the ability to hold charges. The ability for resistors to hold charges is not as strong as a capacitor. Therefore, the capacitance on a manufactured resistor is safely negligible. However, the laser ablated wire does have a certain amount of capacitance because the pads at the end are large in dimension in comparison with the wire in between. Therefore, the pads have a lower resistance while the wire has a relatively higher resistance. The resistance difference causes the wire to act like an open circuit to accumulate charges on one end of the pad. In theory, an RC circuit is connected below.

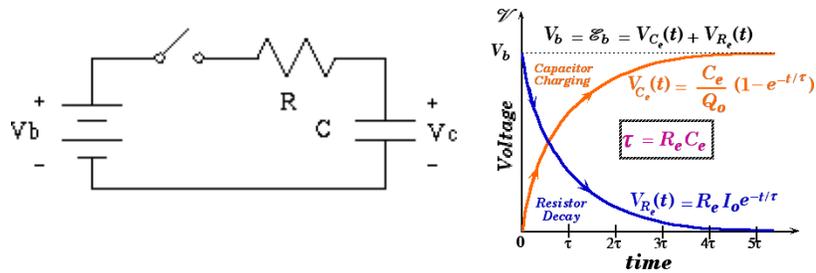


Figure 2.4: RC circuit and its Response

(Left image) <http://www.buchanan1.net/rc.gif>

(Right image) <http://www.ac.wvu.edu/~vawter/PhysicsNet/Topics/DC-Current/gifs/Circuits50.gif>

The voltage response of the resistor and the capacitor is shown in the figure on the right. The equation of the charging curve is

$$V_C(t) = V \left(1 - e^{-t/RC} \right)$$

Equation 7: Charging of an RC Circuit

While the equation for the discharging curve is

$$V_R(t) = V e^{-t/RC}$$

Equation 8: Discharge of an RC circuit

The time constant is the value of the resistance multiplied by the capacitance. It can be calculated easily if both the resistance and the capacitance values are known. From the equation, it is clear that if the capacitance is kept constant, the resistance is proportional to the time constant. This means that it takes longer for the system to charge up if the resistance is high. For an RC circuit, the power input has to last longer than the time constant to turn on the system. This will set a minimum pulse width when testing the wires on the prototype chip.

3.0 White Light Interferometer + Scanning Electron Microscope

Since using femtosecond laser ablation directly on a gold surface is a new IC fabrication process, it is useful to know the surface property of the chip. This information will help guide the future fabrication process by providing calibration knowledge for the fabrication equipments. In order to characterize the prototype atom chips' surface, the two optical based equipments are used: Scanning Electron Microscope, and White Light Interferometer. This section will describe some of the measurements attained from each of these instruments and make a comparison between the two.

3.1 White Light Interferometer

The White Light Interferometer is located in the ICICS building at room X027; contact information is in the appendix. This equipment utilizes the wavelength of the white light to measure the patterns on a surface. The surface of the sample has to be reflective for the equipment to work. The light is sent through two optical paths, with one being the reference and the other will bounce off the sample. When the two paths recombine, the difference in physical distance will cause a difference in optical phase. A Fringe pattern is then formed based on the optical phase difference and an image can be formed. The Wyko NT1100 white light interferometer has a vertical measurement range from 0.1 nm to 1 mm and a vertical resolution of less than one Å.

The training for the Wyko takes about two hours. A brief description of the measurement process is documented here; the detailed testing protocol is in the appendix. Before loading the chip onto the platform, the platform needs to be lowered. Once the sample is loaded, the platform can be slowly lifted to get a clear image. The intensity of the graph also needs to be adjusted. The platform can be tilted to generate either a vertical or horizontal pattern of interference fringes. This process is repeated several times until a clear image is formed. From the software, a cross section profile graph is generated as shown; the X profile is of interest. A tool on the software can help measure the widths from the profile graph.

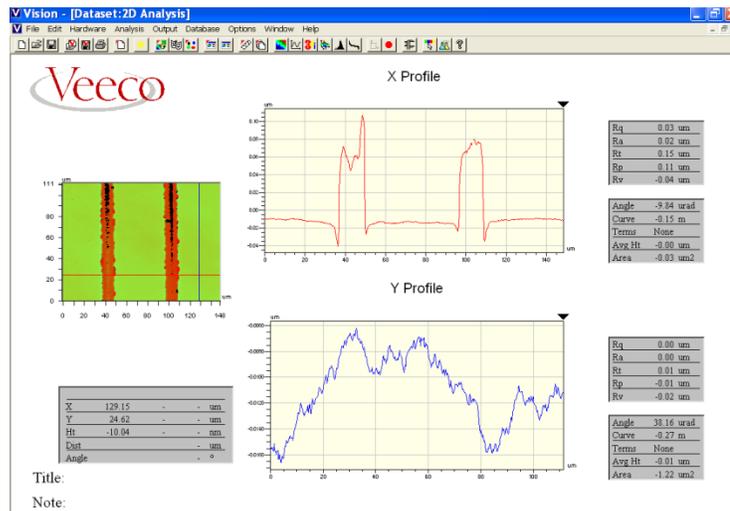


Figure 3.1: White Light Interferometer Cross section profile graph

From the X profile above, it is shown that there are slight bumps on the edge of the cuts. These are speculated to be caused from the laser ablation process in which the etched away gold is building up at these edges. The data for the wire widths measurements are listed below.

	Measured Micro-Wire Widths (μm)				Programmed Widths (μm)		
Chip1	52.5775	20.0074	9.3058	14.4239	50	20	10
Chip2	46.994	93.0576	192.9084		50	100	200
Chip3	46.9941	19.0768	6.0487		50	20	10

Table 4: White Light Interferometer Data: Measure Micro-wire Widths

These measured widths above can be compared to the programmed / intended widths during the manufacturing process. In order to compare them, the measured widths are plotted against the programmed widths. The plot is generated by taking 5 data points from chip 2 and chip 3 which are considered as the good chips. Chip 3 has a wire which was cut twice by the laser and its width is 6.0487 μm which is only 60% of the programmed width (when the cut is wider, the wire which is between the cuts, is thinner).

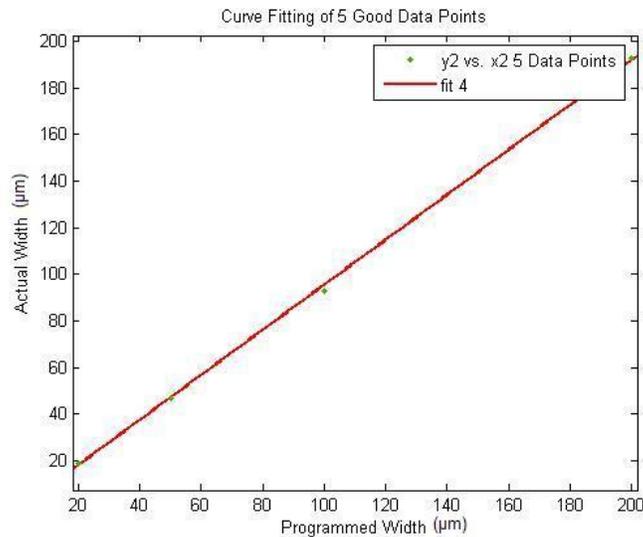


Figure 3.2: Plot of the Measured Width vs. the Intended Programmed Width

The fit is as follows:

Linear model Poly1:	Goodness of fit:
$f(x) = p1*x + p2$	SSE: 4.796
Coefficients (with 95% confidence bounds):	R-square: 0.9945
$p1 = 1.002 (0.05693, 1.947)$	Adjusted R-square: 0.989
$p2 = -2.684 (-32.58, 27.21)$	RMSE: 2.19

The slope is almost unity which indicates that the increment rate between intended width and the measured width is the same. This means, if the laser cut one wire accurately, the rest of the wires will also be in accordance with the programmed width as long as the laser uses the same settings as before. The intercept of the fit is $-2.684 \mu\text{m}$. This is a possible indication of backlash during the movement of the laser platform. This fit information can be used to calibrate the platform for future laser ablation processes.

In addition to width information, the white light interferometer can provide the surface images of the chip. These images can be compared to one another to determine the quality of the wires. If the edge and surface properties of a wire are satisfactory, its settings during manufacturing can be focused on and refined based on these information.

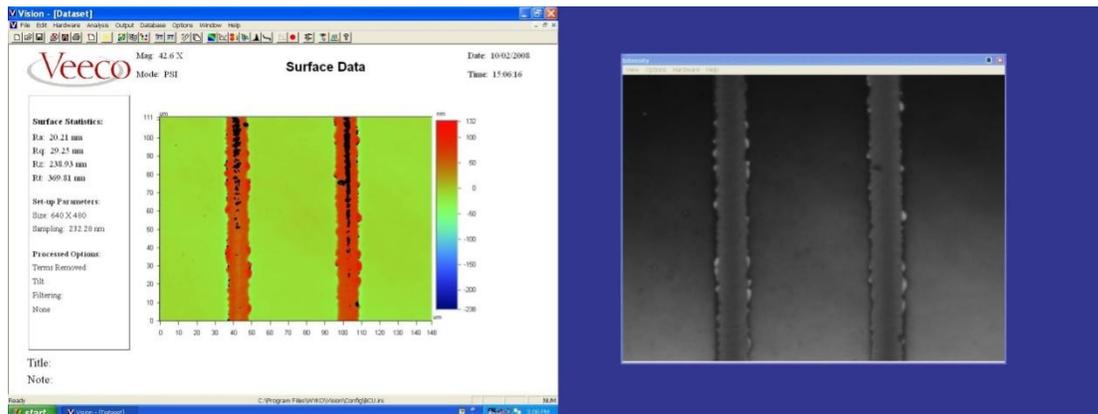


Figure 3.3: White Light Interferometer Image for the Chip Surface

The green region between the orange lines indicates the wire which is $46.99 \mu\text{m}$ on the 3rd chip. The orange lines indicate the laser ablation trenches. The black area in the middle of the trench is indicating a large depth which is the result from overpowered laser ablation. The substrate is damaged which causes the surface to be non-reflective, and thus dark in the colour image. The image on the left is interpreted by the software and the right is the actual image.

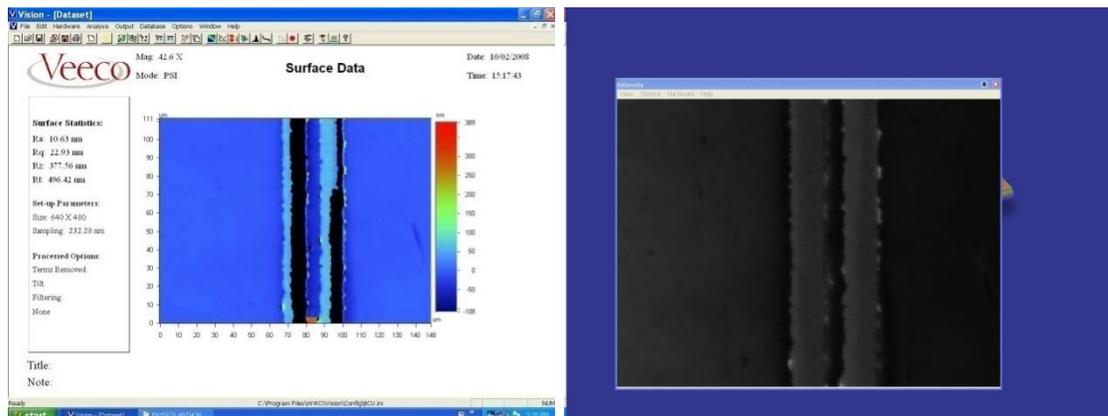


Figure 3.4: White Light Interferometer Image of the Double Wire

The image above shows the thin wire on Chip 3. As mentioned above, the black color indicates damaged non-reflective substrate underneath the gold. The dark blue region in between the light blue lines represents the wire. According to the sponsor who made the chip, this wire was cut twice by the laser which is why the wire is much narrower than the desired width.

3.2 Scanning Electron Microscope

The scanning electron microscope is located Room 45 of the basement in the EOS building. It can be rented for \$ 30 per hour and the contact person is Dr. Mati Raudsepp. Additional contact information on the SEM will be provided in the Appendix.

The SEM has a vacuum chamber for the sample and an electron gun that shoots a high energy beam of electrons toward the sample. The electrons bounce off the surface atoms of the sample to generate signals that contain the surface topological information. It is then picked up by either an X ray detector or a back scatter detector inside the chamber.

Before putting samples inside the SEM, they have to be treated with a carbon paste to make the sample surface conductive. This will drain the electrons away from the surface of the sample. Since the sample's surface is gold, a carbon paste sticker can be placed below the chip and four strips of carbon paste can be used to link the sticker to the top gold layer. If electrons accumulate on the sample surface, it will blur the image. In the SEM images, the whiter areas are indication of electron accumulation.

Since the chamber of SEM is always kept at vacuum condition, pressure has to be increased before the sample can be put in. Once the chamber is opened, the platform of the holder has to be adjusted to the right position so that the sample does not interfere with the detector. The software that controls the SEM is installed on the computer next to it. Detailed procedure of using the SEM can be found in the Appendix.

SEM Images were taken on the first chip, which is also known as the bad chip. To figure out the length scale on the image, information on the width of the wire needs to be utilized. Knowing the width of the wire in each picture, one can draw a line that connects the left and right edge of the gold wire. This line is shifted to start from the left side of the image and is copied and pasted to increase the length of the wire until it reaches the right side of the graph. This gives an estimation of the width of the picture. Then the width of the picture is divided by the number of pixels in the graph to give an estimation of length per pixel.

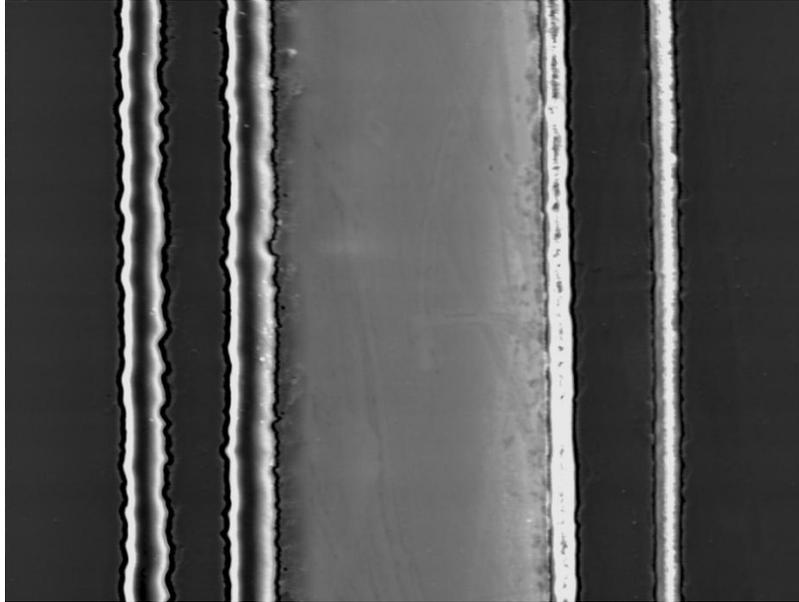


Figure 3.5: SEM Image of the Double Wire

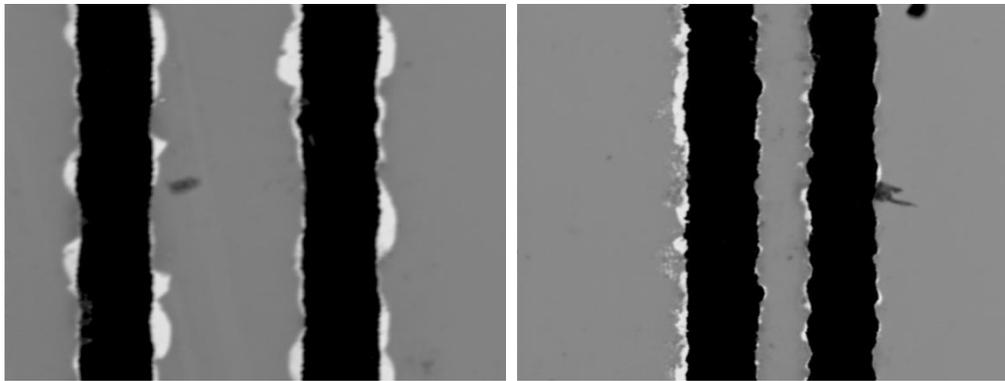
The image is divided into smaller portions featuring the wire ablation edges for analysis. The analysis is done with Matlab. First, the x-direction pixels are separated into regions by inspecting columns of the image. The separation process is carried out by the following lines of code:

```
image = rgb2gray(imread('20UM.jpg')); % load the image and convert it into a matrix of numbers.  
imshow(image(1: 1936,LBOUND:RBOUND)); % show the image column and adjust the pixels.  
image1 = image(1:1936,LBOUND:RBOUND); % transfer part of image into image1.
```

This process is repeated until the data to be analyzed is picked out. The following four portions were picked out featuring the ablation edges.

Using the code attached in appendix and the isolated data shown above, the mean and the variance of the edge of the cut is estimated below. The units are all in micrometers (μm). The mean values starts from the left edge of the graph.

On the first chip, there are two sets of wire that were cut next to each other by the laser. The original goal was to make a $15\ \mu\text{m}$ wide wire. However, during the ablation process, it is suspected that the laser didn't cut through the gold layer. Therefore, the operator decided to repeat the process again with a lower power rating of the laser. However, once observed by the SEM, it was found that the laser didn't cut the same place twice. Instead, a new wire is born $50\ \mu\text{m}$ away. The interesting observation is that the edge cut at lower power is much smoother than the edge cut at normal power.



(a) Smooth, Low Power

(b) Rough, Normal Power

Figure 3.6: SEM Image of Edge Roughness

The left one on top is smoother while the right one on top is rustier, and it can be shown by the following analysis in Matlab.

Left Wire Image (Smooth)

	1 st Left Edge	1 st Right Edge	2 nd Left Edge	2 nd Right Edge
Mean	7.1341	13.319	27.624	34.123
Standard Deviation	0.30873	0.13093	0.17833	0.18239

Table 5: White Light Interferometer Data: Mean & Deviation of Smooth Edges

Right Wire Image (Rough)

	1 st Left Edge	1 st Right Edge	2 nd Left Edge	2 nd Right Edge
Mean	28.671	39.968	49.286	59.751
Standard Deviation	0.28344	0.44794	0.39991	0.34422

Table 6: White Light Interferometer Data: Mean & Deviation of Rough Edges

By this data, the width of the left wire is:

$$\text{Width} = \text{Mean of 2}^{\text{nd}} \text{ Left Edge} - \text{Mean of 1}^{\text{st}} \text{ Right Edge} = 27.624 - 13.319 = 14.305 \mu\text{m}$$

and the width of the right wire is 9.318 μm wide. The values are in agreement with the values achieved from the White Light Interferometer which were 14.4239 μm and 9.3058 μm . The standard deviation values in the right wire are larger than the values in the left wire which indicates that the cut on the right is more rough than the left cut.

The reason why the first chip is called the bad chip is because the laser didn't cut through the gold layer in some parts. The image below shows an example of a bad cut that features the pad on the end of one wire. The laser cut is black in color and the other areas represent the gold. The black line is broken at the bottom right part of the graph and is discontinuous on the bottom left area on the graph.

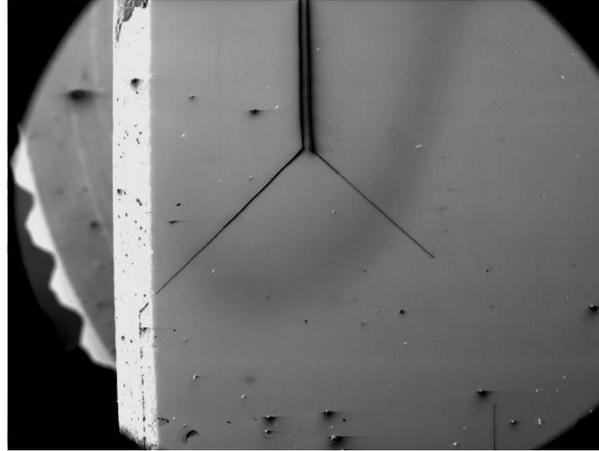


Figure 3.7: SEM Image of Chip 1's Connection Pad

From the SEM image, one could see that the MgF layer on top of the gold is shattered on the edge of the cut. Since the image is produced by electrons bouncing off the sample's atoms, different atoms would produce different signals strength that are interpreted as different colors in the picture. The color on the area is generally gray except on the edges because the gold layer on the edge is exposed to the detector. Materials of higher conductivity usually result in a brighter color while non-conductive materials are darker. This explains why the black line represents the laser ablation. It is because the SiO_2 Layer underneath the gold layer is non-conductive.

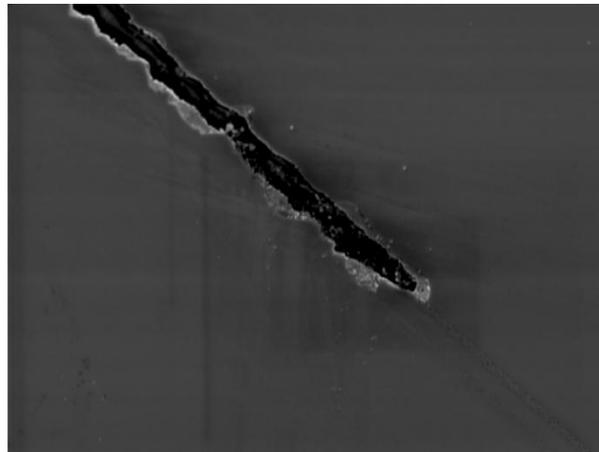


Figure 3.8: SEM Image of Stopped Cut on Connection Pad

4.0 Profilometer

In order to observe the surface characteristics of the prototype chips, the Profilometer was used. The Profilometer is located at the Nanofabrication Facility on the fourth floor of AMPEL at UBC. The particular Profilometer that was used is the travelling probe Profilometer. It is an instrument designed to measure the surface profile by running a stylus across the surface of the sample and measuring the vertical movements of the probe. The vertical resolution of the device is in the nanometres.

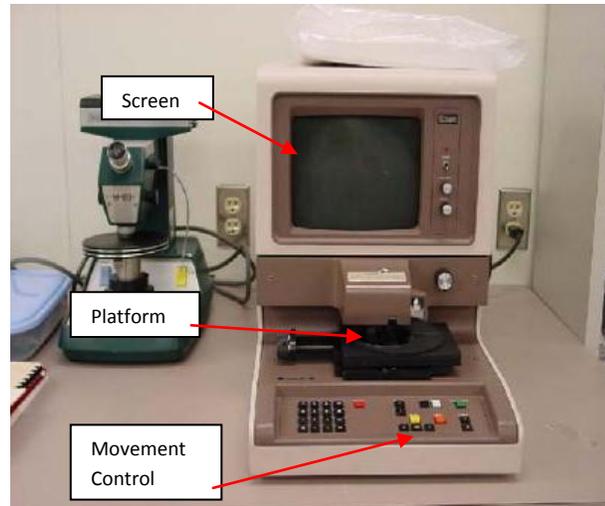


Figure 4.1: Profilometer at AMPEL clean room

Since the facility is a clean room laboratory, the experiment was carried out under the guidance of Dr. Alina Kulpa. A brief description of the testing protocol is documented here. Before placing the sample on the testing platform, make sure the wafer is removed from the platform. When placing the chip on the platform, make sure the wire is aligned towards the device such that the direction of the stylus probe's movement (left right) is perpendicular to the wire (Figure 4.2). This will allow the stylus probe to run across the wire during its measurement and provide data on the depth profile of the cross section across the wire. After placing the chip onto the platform, the stylus tip needs to be zeroed by lowering the tip to just barely touch the chip's surface. Once the movement settings are entered, the tip would move across the chip and measure the depth.

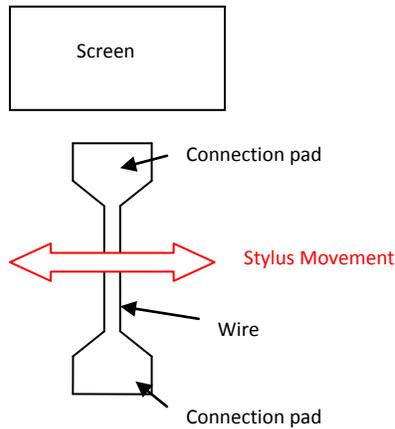


Figure 4.2: Wire aligning

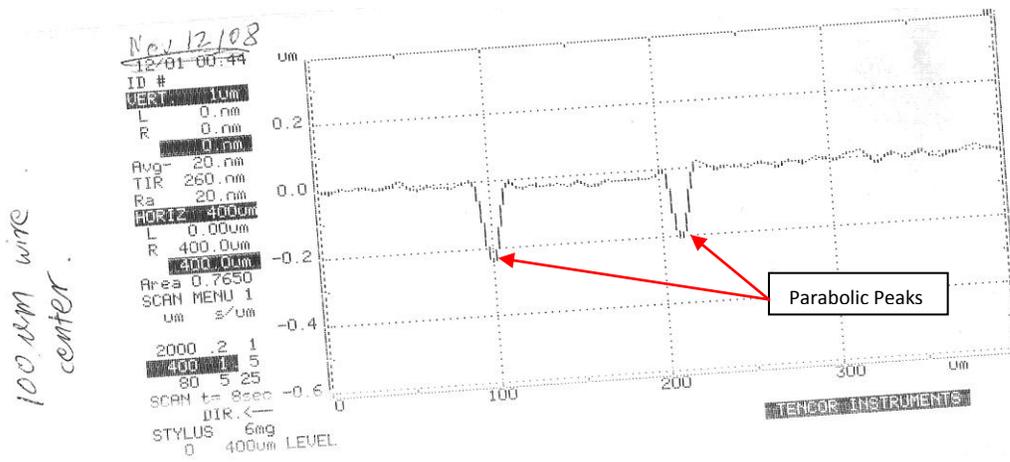


Figure 4.3: Depth profile Measurement: Chip 2 100μm

The sample tested was the second chip's middle wire (100 μm wide) and the measurement result is shown above in figure 4.3. From the image, one could see that each division is 100μm wide with 25 dots. The distance between the two parabolic curves is

$$27.5 \text{ dots} \times \left(\frac{1 \text{ division}}{25 \text{ dots}} \right) \left(\frac{100 \mu\text{m}}{1 \text{ division}} \right) = 110 \mu\text{m}, \text{ which agrees with the intended width of } 100 \mu\text{m}.$$

The two parabolic-shaped peaks can be interpreted as the laser cuts on the chip. However, this graph shows that the bottom of the cuts is parabolic, and resembles the tip of the stylus probe. It suggests that the stylus does not reach all the way to the bottom of the trench, because it is blocked by the edge of the trench as it is lowering. Width readings from the white light interferometer have suggested that the trenches to either side of this wire are 14.19 μm and 15.13 μm. According to Dr. Kulpa, the radius of the stylus tip is 12.5 μm. Since the stylus does not reach the bottom of the cut, the depth of each cut is still unknown.

The image below is an enlarged image which focuses mainly on the right cut. The cut is shown to be 20 μm wide which does not agree with the result from the white light interferometer. This difference in value is probably caused by the size of the stylus. Although the

width may be less accurate, the bumps on the edges do provide valuable information. Since the laser ablated the gold surface by instantaneously heating up the region, the edge of the cut may not be smooth from the piling of the gold molecules that are etched away. Although the stylus couldn't go into the cut trench, it can detect and surface roughness on top of it of the gold layer. Even though the depth information is not very convincing, it is still useful for comparison especially the width information of the trench.

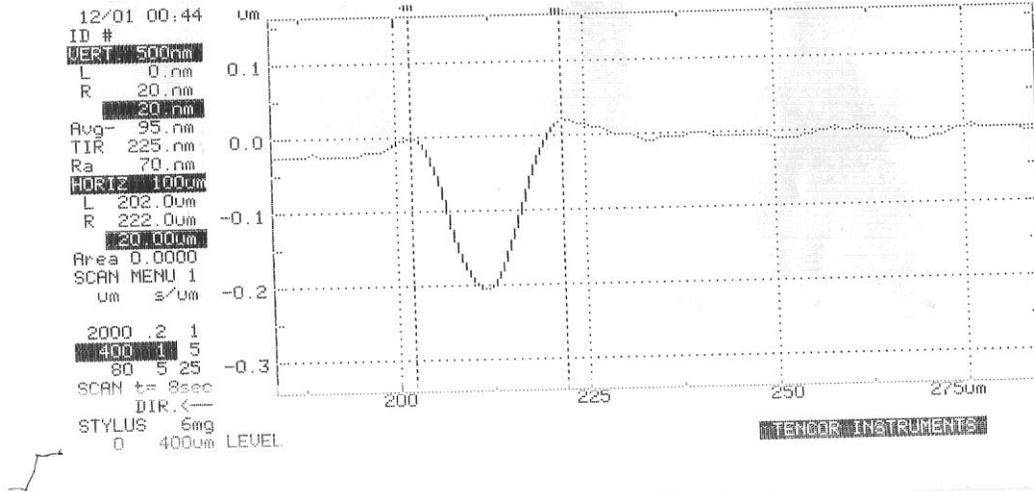


Figure 4.4: Depth profile Measurement: Chip 2 100µm

5.0 I-V Characterization

This section of the report discusses the electrical characterization of the micro-wires on the prototype atom chips. The subject of interest is how the width affects the resistance. Since this project is just one of the many preliminary steps in building an atom trap using atom chips, there is also an implication to test the limits of these prototype chips. Limits such as the amount of current that can be passed into the wire, and the heating effects that may occur when reaching such limits are addressed in this section.

5.1 Preliminary Testing at the Mina Lab

Before plunging straight in designing and building an original apparatus to get the I-V characteristics of the atom chips, the APSC 479 group looked to the expertise of Dr. Mario Beaudoin who is knowledgeable about the testing equipments used throughout the UBC campus. He recommends the chip testing equipment in Dr. Chrostowski's Lab. A short report was written on the data collected at Mina, and it is attached in the appendix.

5.2 Final Testing Apparatus Design

The key objective of the testing apparatus is to provide a stabilization bench for the prototype atom chips while allowing accessible external electrical connections to the wires on the chip. Some design requirements are to allow for the variable physical dimensions of the chips (1/2" to 2" in length), to allow for the removal and securing of the chip with ease, to allow switching between the testing wires, and to provide delicate electrical connections with the pads of the testing wires.

There is an apparatus from the Microsystems and Nanotechnology (Mina) lab in the Kaiser Building of UBC that is used by the Mina group to test the chips that they fabricate. Their apparatus is shown in figures 5.1 & 5.2 below.

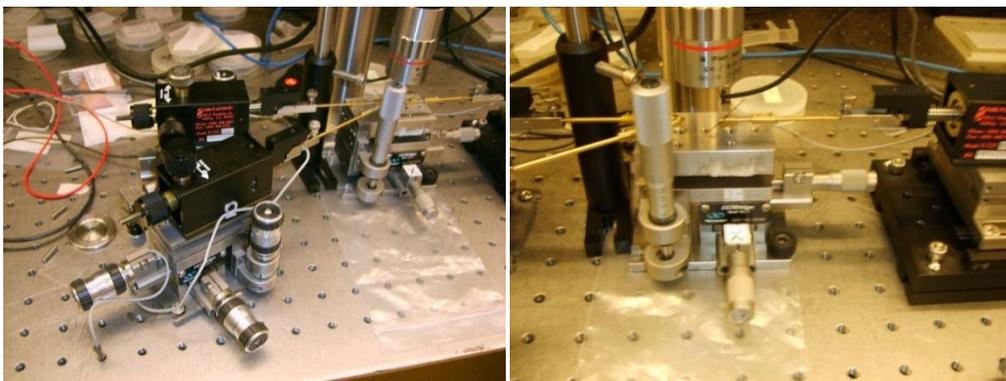


Figure 5.1 & 5.2: Mina Lab Chip Testing Apparatus

The Mina Lab apparatus consists of three x-y-z translation stages. The center stage is for the sample where there is a camera attached to a microscope to help position the sample. The other two stages are to position the actuating spring loading pins that are responsible for making the electrical connections to the sample. These pins are subsequently connected to a

function generation, and a programmable digital multimeter for recording the I-V data of the sample chip. The specific equipments are the Keithley 2602 System Sourcemeter and the Signatone SE-T pins.

With the permission of Dr. Lukas Chrostowski, the manager of the lab, some preliminary testing of the three prototype atom-chips was performed by the visiting / post doc student Mark Greenberg at the Mina Lab. The discussions and results from these measurements are documented in the next section.

After discussing the results of the preliminary testing from the Mina Lab with the project sponsors, they noted some of the limitations. The most notable limitations are that the test performed at Mina uses a two-point contact technique and that the maximum current input from the function generation is programmed to 100 mA. A four-point contact technique is strongly advised by the project sponsor and they would also like to test the limits of the chip with higher currents than 100 mA. In order to incorporate the four-point contact technique and more flexible input signals for the I-V characterization, a testing apparatus needs to be designed and built.

By adopting the design of the Mina chip testing apparatus, two translation stages from the sponsor's labs are used. These translation stages operate with a range of 3 mm in the three principle directions. The translation operates with a power screw using three separate micrometers which allow for fine control when the probe is approaching the wire connection pads on the atom-chip. Instead of designing the probes like the pins used in Mina, an extra arm structure on top of the translation stage is designed by making use of some existing clamps and support rods. The probing pin is then mounted on the rod that is reaching down by locking a small piece of PCB between two nuts. The notable feature of the arm structure is that the reach is adjustable in two directions: one direction for lowering (z) and one direction for moving towards (y). The purpose of this reach is to coarsely approach the wire connection pads on the chip while the micrometers of the translation stage accommodate the finer approach. It is also a precaution of protecting the chip because approaching with the micrometers can allow the probe to just touch the surface of the connection pad and reduce the possibility of scratching the surface. Another notable feature is that the two support rods can rotate. Once the probing pins are aligned (shown later), further rotations may not be desirable. The extra clamp at the middle is added because when the two black screws are loosened for moving the arm, the structure will not rotate.

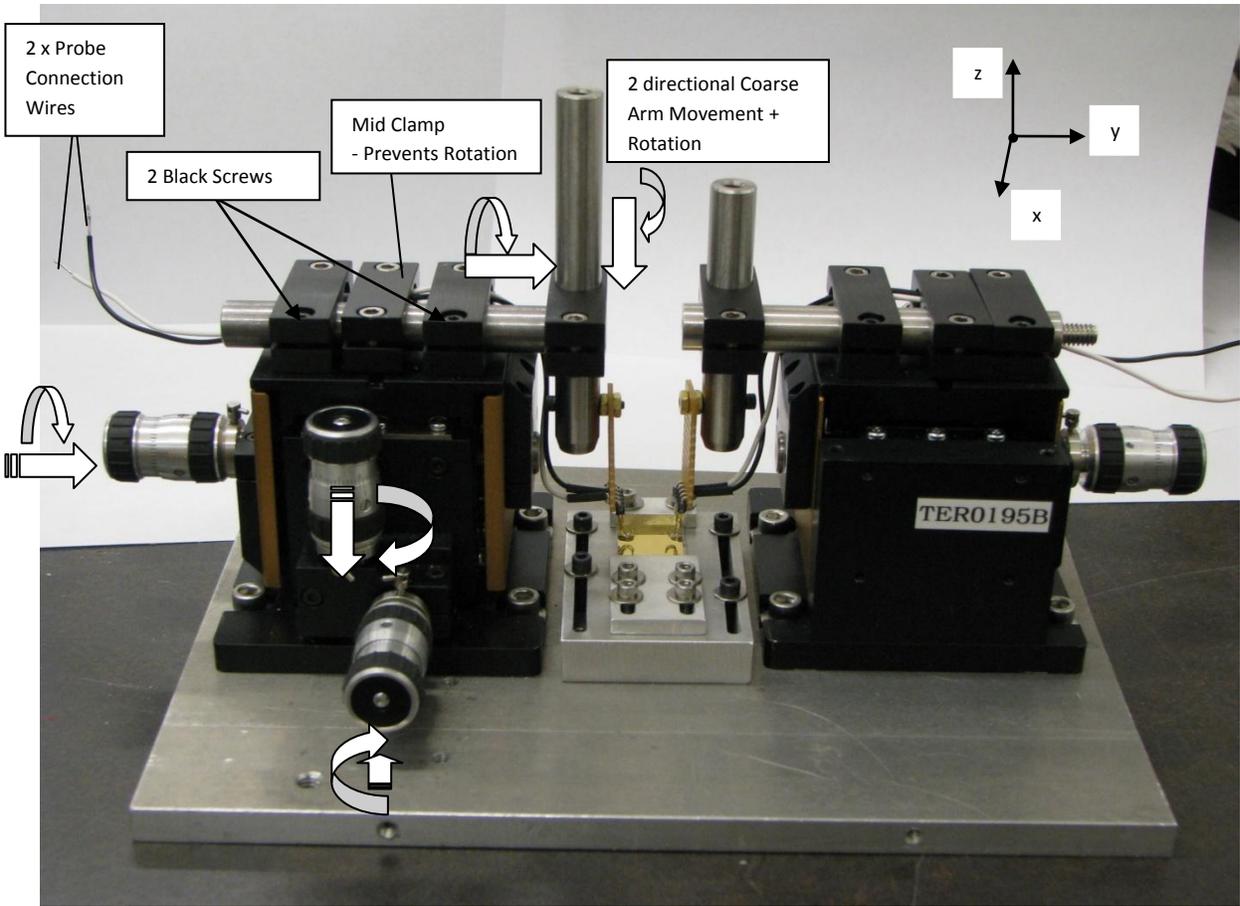


Figure 5.3: Testing Apparatus Manufactured for the Project

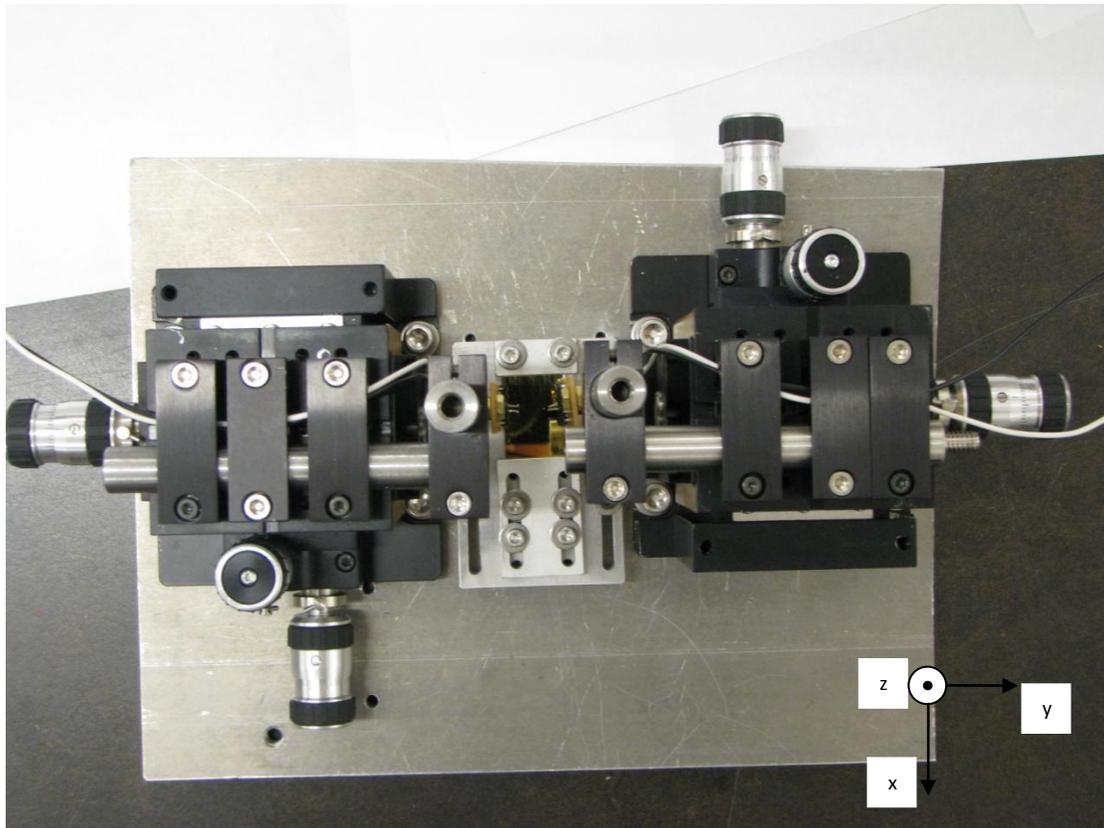


Figure 5.4: Testing Apparatus Top View

The probing pins are designed by securely placing a piece of four right angled male connector pins onto a piece of PCB. Even though only two of these male connector pins are needed, the extra pins provide support on the PCB. From the back of the PCB, two long wires are soldered on two male connector pins in the middle. These wires are for external electrical instruments to connect to the probes. At the other end of these two male connection pins, two wires bended into a hook are used as the probe stylus. The hook design allows for slight deflections as it is being lowered onto the chip with the micrometer. Not only does the deflection protect the surface of the chip, but the elastic nature of this design will allow a larger contact area between the tip and the chip wire pad. This hook style tip is much easier to form an electrical connection than a stiff tip.

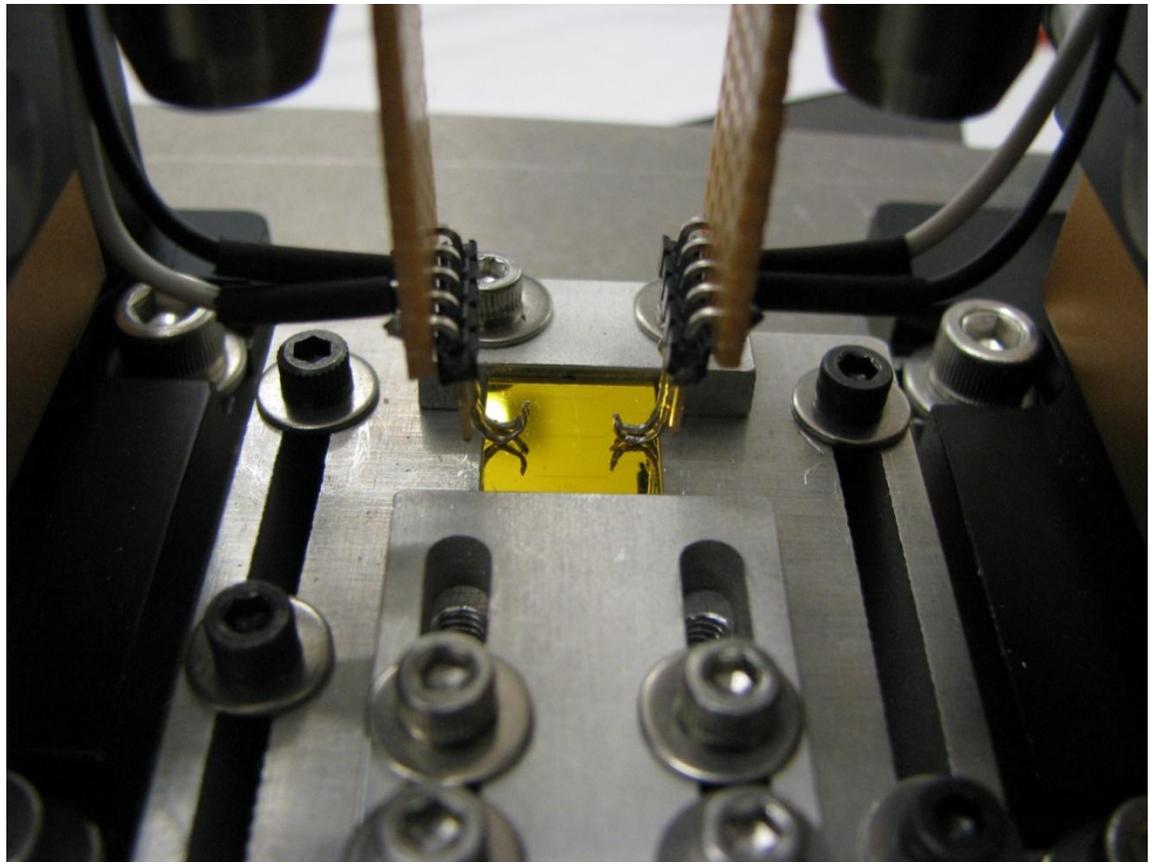


Figure 5.5: Testing Apparatus Probing Pins

5.3 Experimental Equipment

Besides the testing apparatus described in the previous section, the electrical testing of the prototype chips also requires the following: an oscilloscope, a current source, a set of current triggering instruments and a multimeter.

The oscilloscope is the Tektronix TDS 2004. It has four channels and is capable of sampling the signals up to 60 MHz. The data from the oscilloscope can be uploaded onto a computer for analysis. The oscilloscope uses the RS-232 serial port and a RS-232 to USB connector is required to make the connection. By installing the software from the CD in the oscilloscope package, the oscilloscope screen images and waveform data can be retrieved with the Tektronix OpenChoice Desktop application.

The current source used is the Laser Diode Controller (LDC500). The LDC500 can either be used as a constant current source or it can be pulsed with triggering instruments. The triggering instruments and the current source will be described in further details. The multimeter is mostly used for reading the resistances and checking the connections and most typical multimeter will suffice. One of the multimeters used is the FLUKE 79 Series II Multimeter.

5.3.1 Current Triggering Instruments

The current triggering instruments consist of the BK Precision 4011A 5MZ Function Generator and the Interstate Electronics Corporation (IEC) F33 Function Generator. The BK Precision function is set to send long square waves at the lowest frequency of 0.4 Hz. This is shown as the orange wave in the diagram below. The output of this low frequency wave is then used to trigger the F33 Function Generator. It is set up such that the rising edge of the long square wave will trigger a pulse on the F33 Function Generator. The output of the F33 Function Generator is the blue wave in the diagram below. With this setup, it is possible to generate a pulse with a width of 5 μ s. However the smallest width taken for the data analysis was 50 μ s. A key goal for setting up the system like this is to separate the time length between each pulse. The intention of having such lengthy intervals between pulses is to make sure there is ample time for the system to cool down after the heating effect caused by the pulse. It would become troublesome if the effect from heating still remains when the next pulse hits. The voltage peak to peak amplitude of the blue pulse is also important because that determines the current output of the LDC500.

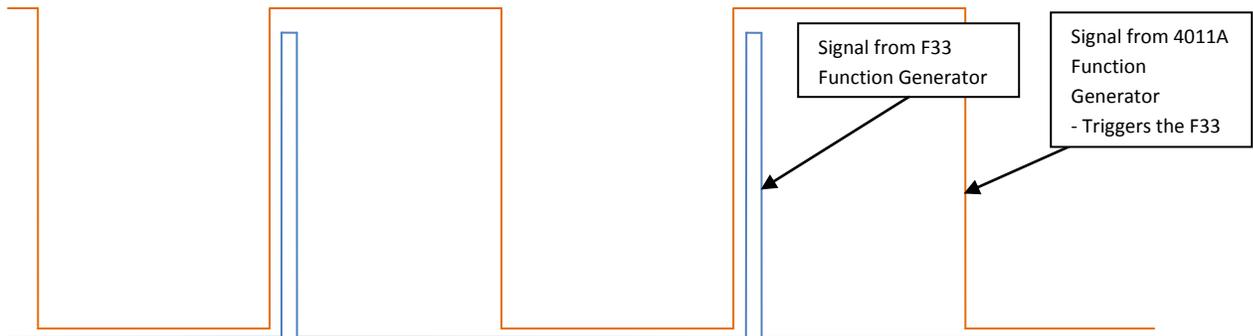


Figure 5.6: Testing Apparatus Probing Pins

Some operational notes about the setup will be mentioned here; references are made on the figure below. The output of the BK Function Generator will be viewed using Channel 1 of the oscilloscope and its 'Mos' is connected to the trigger of the F33. The trigger level of the F33 will be using the "Trigger Mode". Both the function generator waveforms will be using square waves.

Before proceeding to the actual testing of the chip, it is a good idea to determine the amount of current and the time to which the current is provided (width of the pulse). The width of the pulse is adjusted by the two knobs: Frequency Level and Duty Cycle. For widths of 10 μ s, the frequency level of 100 K can be used. For widths of 100 μ s, the frequency level of 10 K can be used and so forth. The maximum width of the pulse using this setup is about 500 ms which uses the frequency level of 10.

The voltage of the F33's signal is controlled by the two knobs labeled as voltage level below. For the coarse voltage level knob, the levels 0.1 V, 0.3 V, 1 V, 3 V and 10 V are available. The fine voltage control knob expands or contracts the square wave in both directions. It is necessary to use the fine voltage control knob with the offset knob. A good reference is to align

the lower flat horizontal portion of the square pulse with ground. There is a warning light on the F33 function generator. It is observed that whenever the upper flat horizontal portion of the square pulse exceeds 1.3 times the value on the coarse voltage output level setting from the ground reference line, the warning light would light up. In that case, it is advised to lower the offset or turn down the fine voltage output control.

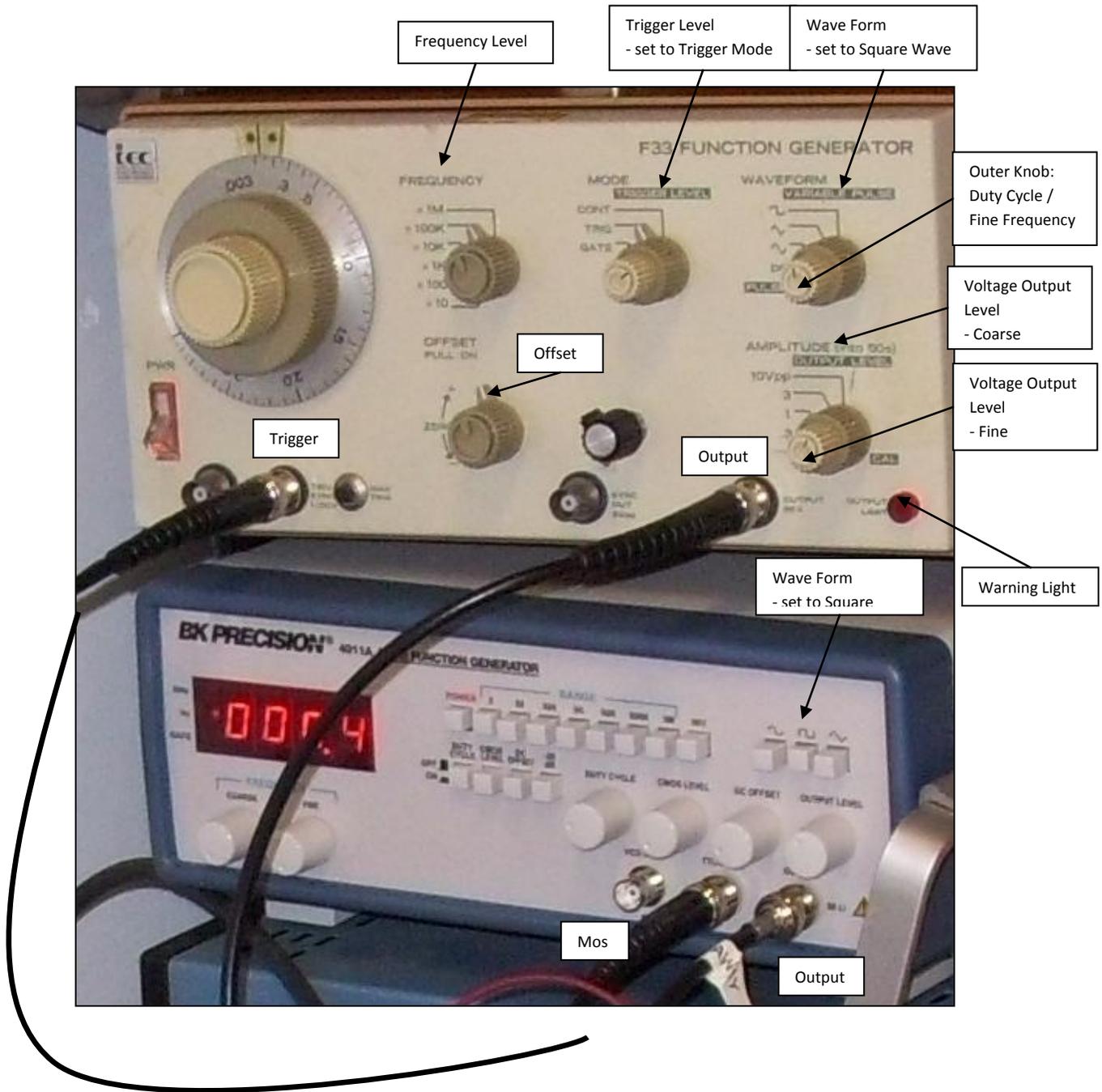


Figure 5.7: Current Triggering Instruments

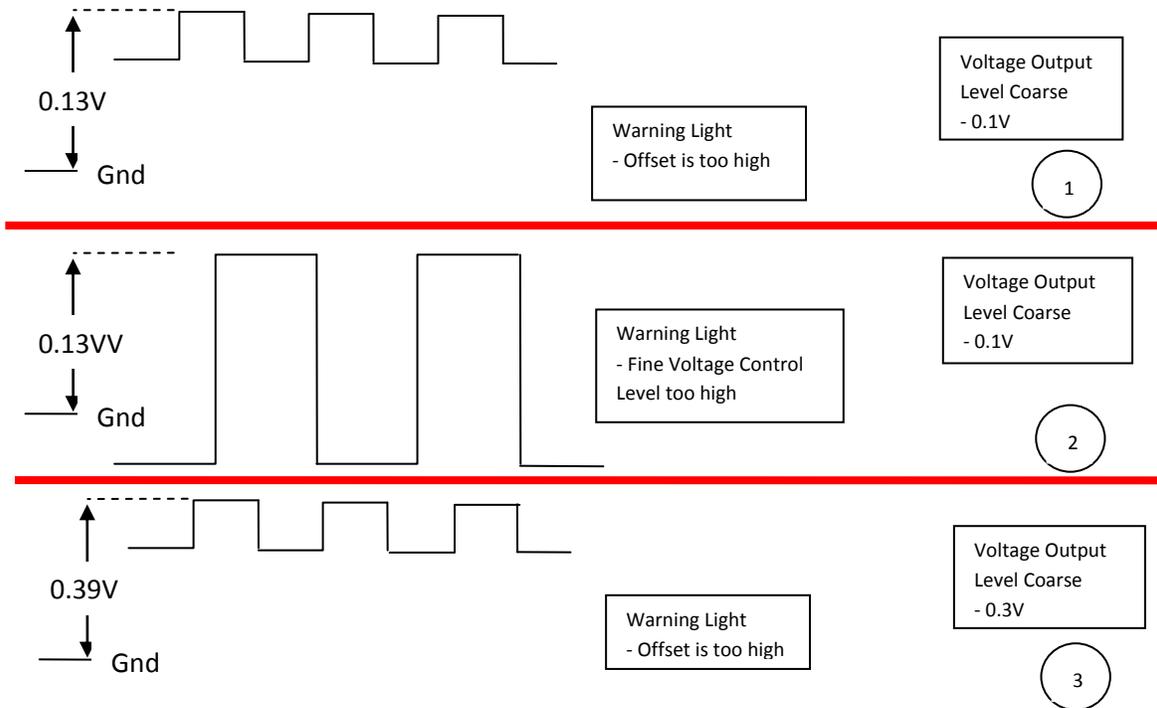


Figure 5.8: F33 Function Generator Warning Light

5.3.2 Current Source

The LDC500 (Laser Diode Controllers) is used as the current source for this project. The control range of this instrument is from 0 to 500 mA. It can either be used as a free running constant current / power source or it can be triggered with the triggering instruments in the previous section. With a pulse controlling the LDC500, the sensitivity is 50 mA / V. A 10 V peak to peak square pulse from the F33 Function generator will cause the LDC500 to output the maximum current of 500 mA. There is a safety output limit of the device which can be adjusted by a small flat head screw driver (labeled limit in the below figure). If the LDC500 is not triggered, its output current can be adjusted with the constant current knob. Even if it is controlled, this current knob can be used to add a constant current offset to the analog current output from the triggering. For this project, the current knob and triggering are not used together.

There is no output from the LDC500 unless it is enabled. The enable button acts as another safety mechanism. The LDC500 can also detect whether the circuit has an open circuit or rather the circuit is drawing more current than the maximum power consumption of 30 W. The open circuit warning will light up accordingly and the instrument will automatically disable.

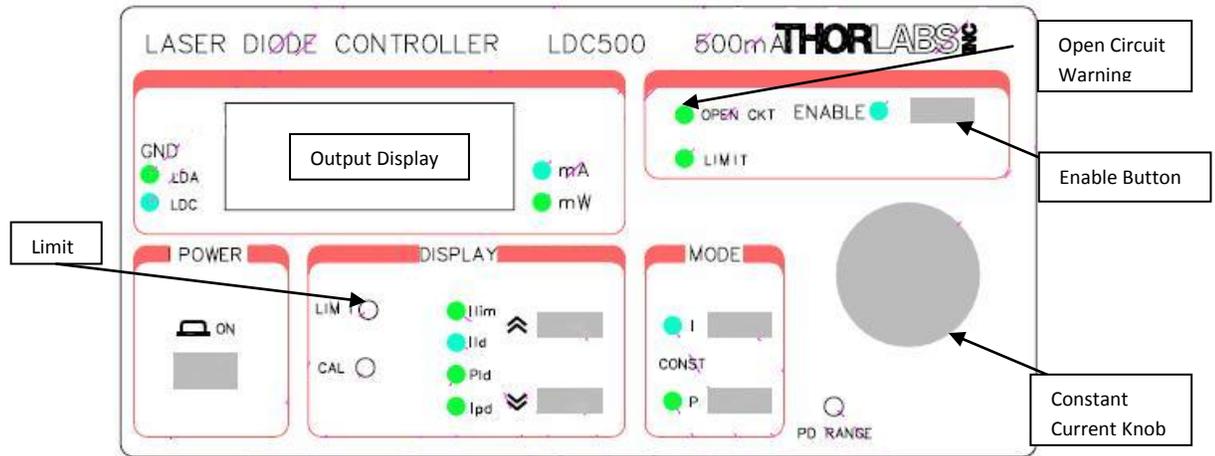


Figure 5.9: Laser Diode Controller 500

The output of the LDC500 is the RS-232 with pins shown below. Pins 1 and 5 are shorted for a safety interlock. The photodiode pins and pin 7 are not used. Pin 8 is soldered to a long red wire (anode) and pin 3 is soldered to a long black wire (ground). In the connection diagram below, the photodiode component is not used, and the laser diode component will be replaced with the wire on the prototype atom chips.

<u>pin</u>	<u>connection</u>
open circuit monitoring, status display:	
1	interlock
5	digital ground for pin 1
laser diode:	
7	laser diode cathode (laser anode is at ground)
8	laser diode anode (laser cathode is at ground)
3	ground for the laser diode
photodiode:	
2	photodiode cathode
4	photodiode anode

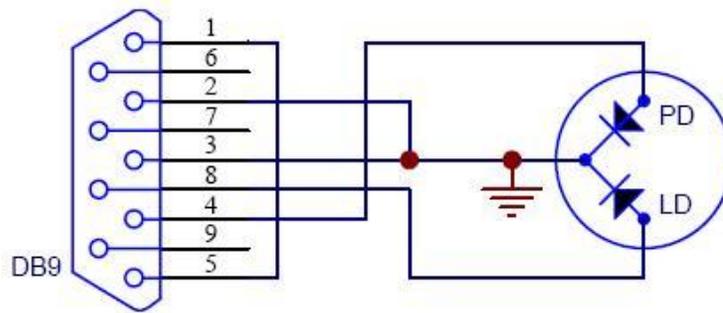
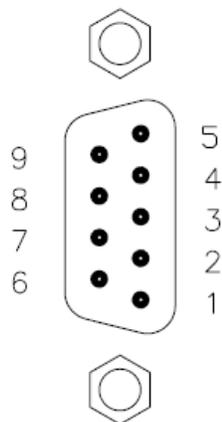


Figure 5.10: LDC500 Output Pins Identification

5.3.3 Equipment Wiring

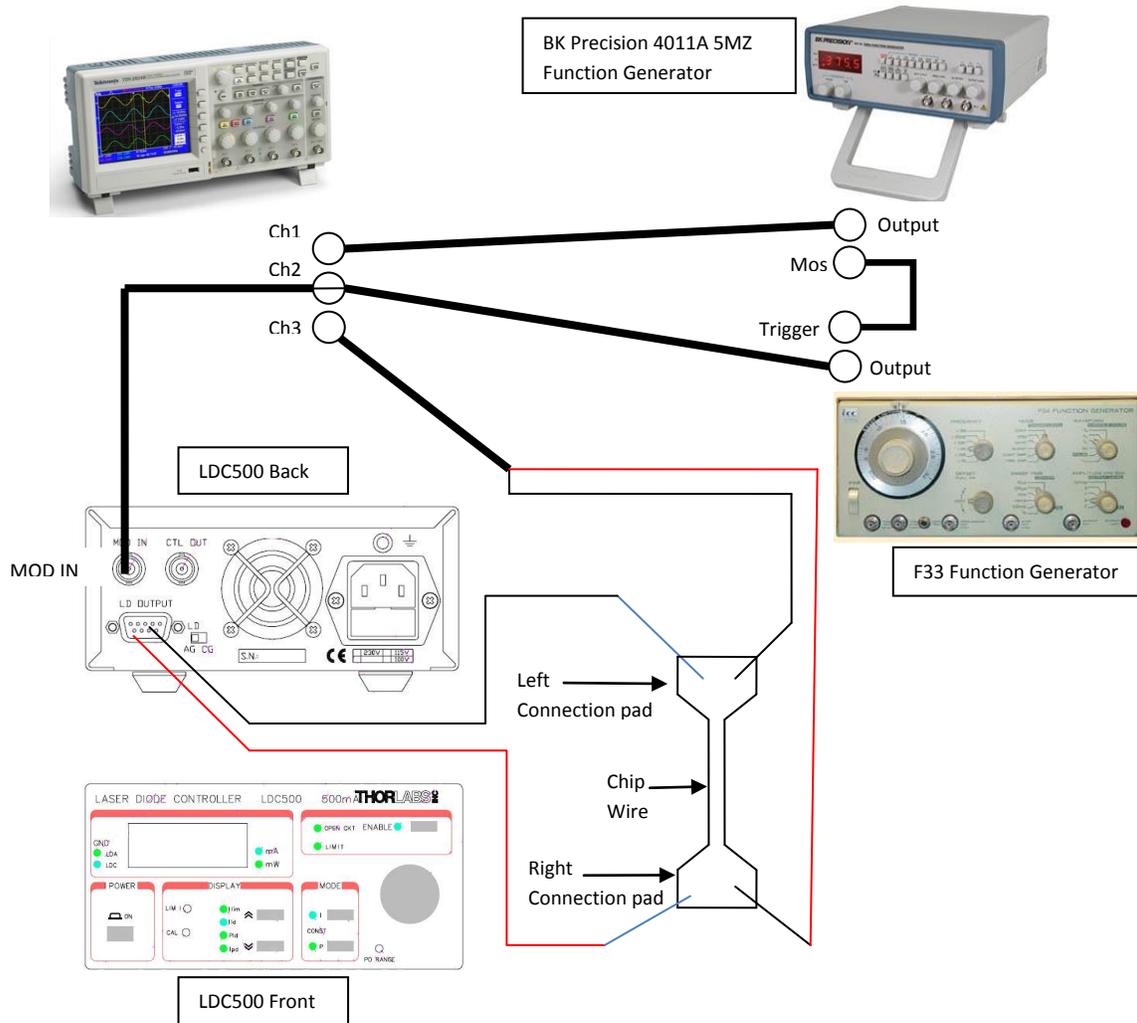


Figure 5.11: Equipment Wiring Diagram

Wiring Diagram Notes:

- white wires are depicted as blue wires
- BNC wires are depicted as thicker lines
- Pay extra care to follow the color scheme otherwise a short circuit will result if the anode from the LDC500 flows directly to the ground of the oscilloscope before the wire

Three channels on the oscilloscope are used. Channel 1 is useful for triggering the oscilloscope. Channel 2 is useful for determining the amount of current to pulse and the duration of the pulse while Channel 3 observes the voltage drop across the wire on the chip. In addition a BNC Junction Tee connector is used at Channel 2 so that the signal can be observed and be used to pulse the LDC500. An actual photo of the equipment set up is shown below.

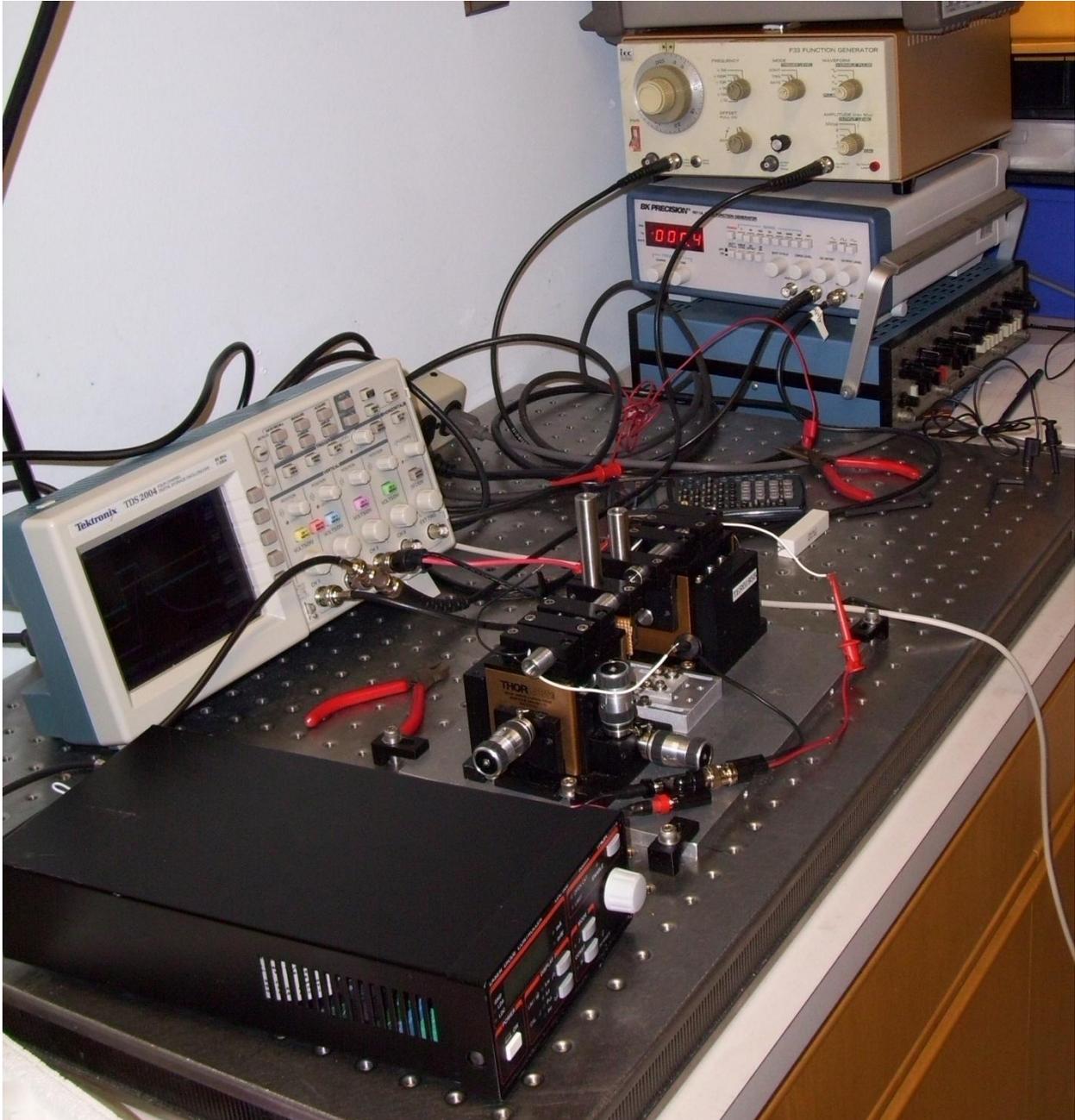


Figure 5.12: Equipment Wiring Photo

5.3.4 Testing the Equipments

In order to verify the information in the specification sheets of the electrical instruments, some tests were conducted. Two high power rated resistors are used to test the equipments before the actual micro wires on the atom chips are tested. The resistors are an $8\ \Omega$ resistor with power rated at 20 W and a $4.7\ \Omega$ resistor with power rated at 11 W. These resistor values are comparable to the resistor values of the micro wires (lowest measured to be $16\ \Omega$ for the thickest micro wire of $200\ \mu\text{m}$).

If the maximum current of 500 mA from the LDC500 current source is put through the 8 Ω resistor, the power is calculated to be:

$$P = I^2R = 8 \Omega \times (500 \times 10^{-3} \text{ A})^2 = 2.0 \text{ W} \ll 20 \text{ W (resistor limit)} \ll 30 \text{ W (LDC limit)}$$

It implies that the resistor can withstand the maximum current output from the current source. Similarly for the 4.7 Ω resistor,

$$P = I^2R = 4.7 \Omega \times (500 \times 10^{-3} \text{ A})^2 = 1.175 \text{ W} \ll 11 \text{ W (resistor limit)}$$

These resistors are tested by sending an increasing current through them with the LDC500 current knob and a multimeter is used to measure the voltage. The voltage versus current graphs are shown below; these graphs are linear as expected. The fit shows that the actual resistances are $8.08 \pm 0.003 \Omega$ and $4.787 \pm 0.001 \Omega$.

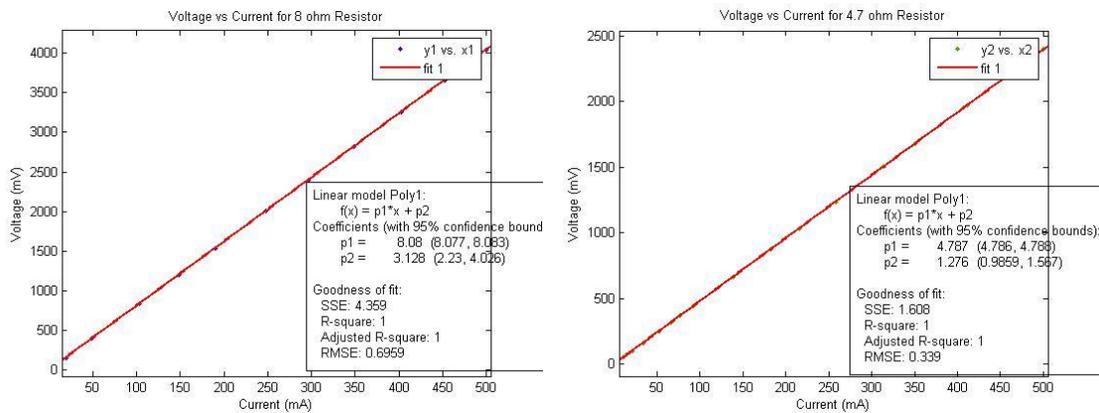


Figure 5.13: Voltage vs. Current graphs for 8 Ω & 4.7 Ω test resistors

When looking at the voltage drops on the oscilloscope, a horizontal voltage line is observed. It is noted that the signal has some noise, and is a thick line with thickness of about 3 mV. It suggests that the resolution of the oscilloscope + LDC500 current + wire system is 3 mV.

The LDC500's sensitivity is tested by sending in known voltages. The pulse from the F33 function generator (channel 2) is set to have a duty cycle of 50% with a low frequency of 0.5 Hz so that the current signal will be on for one second and be off for the next second. This current jump can be seen on the LDC500's display. A one volt signal is tested, and a jump between 0.2 mA and 48.2 mA can be seen. 50 mA is not seen because there is a lag in the LDC500's display and the jump between the currents is rather fast. This current out is also passed through the 8 Ω resistor and observed on the oscilloscope. A 400 mV to 0 mV square output voltage signal is observed.

Short and fast pulses from the F33 function generator are also tested to confirm whether the LDC500 can follow the pulses. The output observed from a 10 kHz input is confirmed to be satisfactory while the 100 kHz input is showing signs of an electrical lag rather than a neat square wave. From these observations, it is advised to use pulse widths of longer than 10 μs.

5.4 Testing Method / Protocol

After wiring the equipments as shown in the previous sections, a chip and one of its wires has to be loaded properly on the testing apparatus before the actual IV testing can begin. Once a micro wire is successfully connected with the electrical instruments, the signals that will be used to test the IV are largely determined by the resistance of the wire. In this section, the general testing method will be described, with a more detailed protocol documented in the appendix.

5.4.1 Chip + Wire Loading

Assuming there is no chip already situated in the testing apparatus, a chip will have to be loaded into the apparatus and one of its micro wires will have to be aligned with the probes. One of the first steps is to make sure the arms structure on the translation stages are not interfering too much (blocking access to screws, etc) in the area between the stages. It is also necessary to lift the probes (+ z), move away from the center between the stages (-y for lower stage and +y for upper stage) and towards one side (-x for both stages) using the micrometers. In other words, the three micrometers are adjusted to their extreme end travel limit of 3 mm.

Clip 1 should always be screwed down to the base piece. Place the chip lying on one side onto Clip 1 and make sure the micro wires on the chip are aligned in the y direction such that both ends the micro wire connection pads are toward the stages. The chip is then secured by placing Clip 2 on the Base and lightly pushing the chip against Clip 1. When screwing Clip 2 onto the base, washers should be used. Once the chip is lying securely in the smaller holder, the base can be placed on the base plate. This holder can be moved in the x direction to align the probes with the micro wire of interest's connection pad. Make sure to align the twin tips of the probe to be just slightly on the -x side of the connection pads because the x travel micrometer is on its -x end limit, and can still accommodate 3 mm of + x travel.

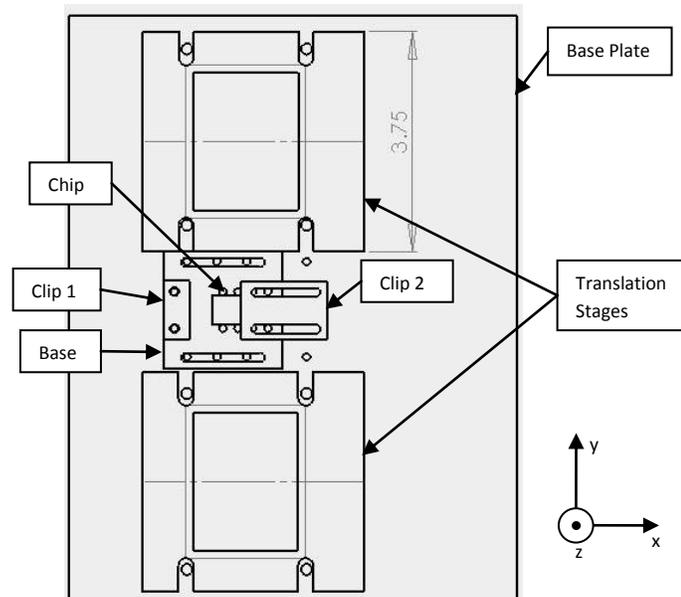


Figure 5.14: Test Bench Chip loading

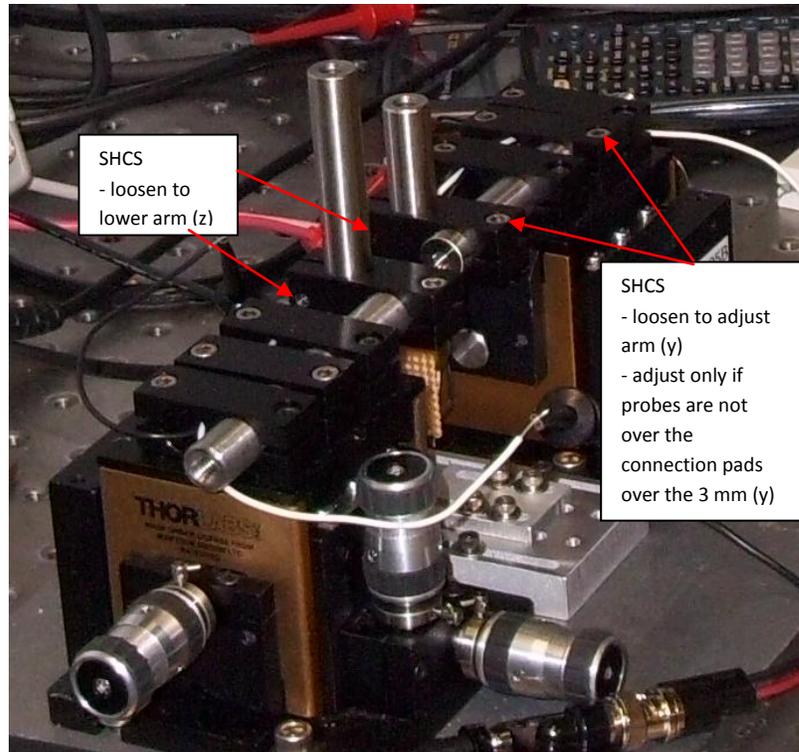


Figure 5.15: Coarse Arm Adjustment

Now that the chip and the chip holder are in place, the arms can move back toward the center. Be sure to only adjust one direction of one stage at one time. For the y direction, it may not even be necessary to use the coarse arm adjustment. It can be used if the connection pads appear to be too far in the y direction for the 3 mm of micrometer travel. The important direction is the z direction. It is recommended to loosen the arm and move the probes to be as close as possible to the chip. It has to move within 3 mm from the surface of the chip with a recommendation to between 1 to 2 mm. In addition, it is important to make sure the probes are still aligned and the arms did not rotate too much during the coarse arm adjustment process.

After the coarse adjustments, the fine adjustments with the micrometers can be used. It is advised to adjust one of the translation stages first before adjusting the other stage. First adjust the x and y micrometers such that the probes are directly over the connection pad. A multimeter should be attached to the pair of white and black wires. The probe tip pair should form a close circuit and display a resistance value as soon as it is connected. Lower the probes using the z micrometer to just barely touch the surface of the connection pad. The probe may not be connected with the first try lowering the probe tips because of the unknown layer of protective magnesium fluoride on top of the gold. With the probe tips touching the connection pad, run the y micrometer back and forth to slightly scratch the surface. From the experiments, a value of around 1Ω should

be observed once a connection is made. If running the y micrometer back and forth doesn't help, do the same for the x micrometer; also try lifting and lowering (z) the probe tips again. The same can be done to the other translation stage until a resistance reading can be read on both sides. Now the resistance value for the micro wire can be read with a two point method by using the multimeter as shown in the photo below.

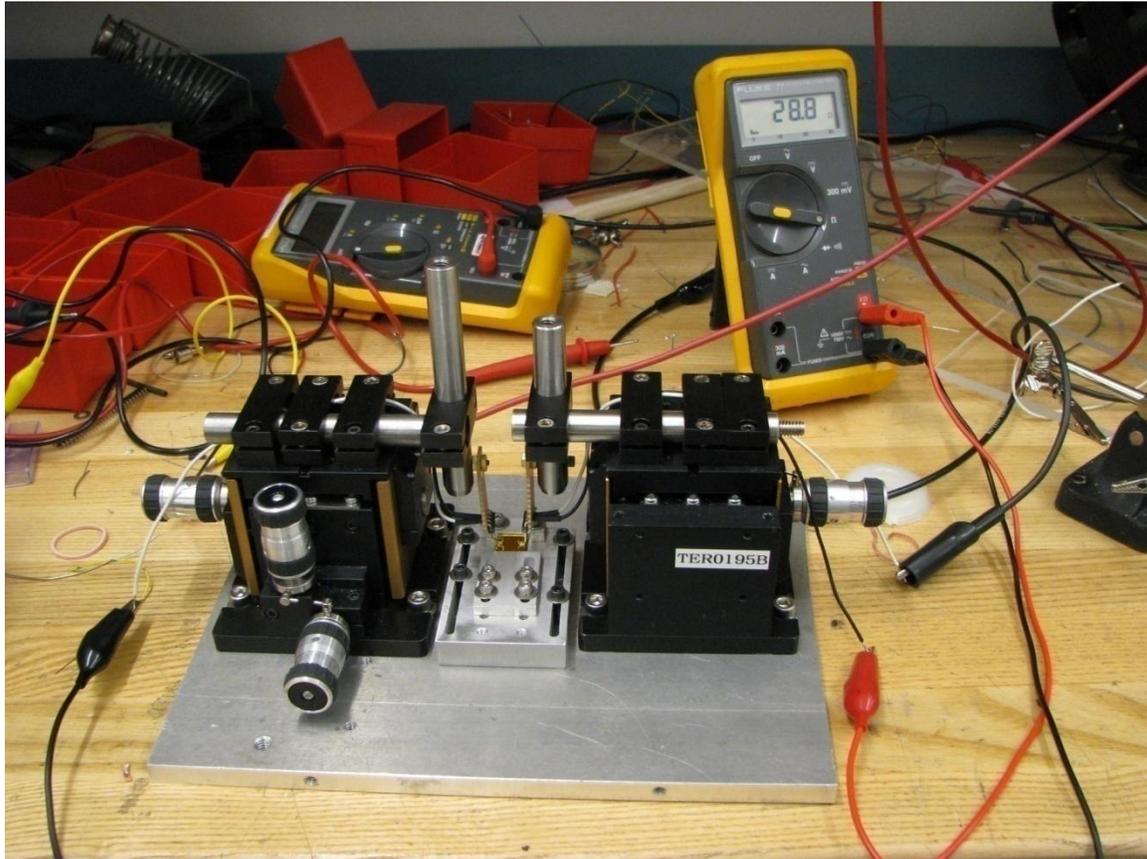


Figure 5.16: Measuring Resistance for the Chip 2 100 μ m Micro Wire

5.4.2 Testing Approaches

There are three prototype atom chips with three micro wires on each one. One distinction between the micro wires is that most of them have different wire widths. Since the three chips were manufactured from the same material, they all share the same depth of gold. The resistance values for the wires are therefore proportional to the width of the wires. The two point resistance value can be used to determine the amount of current to test the chip. The general methodology is to begin by sending very short pulses with currents that are definitely within the limits of the chip (5 mA for 0.1V from F33 function generator), and then increasing the width of the pulses by tenfold each time. For the very short pulses, the electrical system response can easily be observed, and the chip heating factors can be ignored. As the pulses get longer, the electrical and the heating effect can be observed together. The hypothesis is that the electrical response is very similar for long and short pulses, and is focused at the start and end of

the response for long pulses. In the middle of the response, the heating effect is suspected to show a linear rise in voltage. As the wire heats up due to the input of electrical power, the rise in temperature is speculated to cause the increase in resistance through the equation:

$$R = R_0 (1 + \alpha \Delta T)$$

R = new resistance after heating

R₀ = resistance before heating

α = linear temperature coefficient = 0.0034 / °K for gold

Δ T = temperature change

This increase in the micro wire resistance will drive a corresponding increasing voltage drop across the micro wire over time which can be observed and recorded with the oscilloscope. From the oscilloscope voltage data, the resistance information can be generated since the power source is a constant current source. Through this above equation, the temperature rise plot can be generated versus time. A note to pay attention to during the testing is that the sponsor has mentioned that heating up the chip to 100°C may damage the chip. From the equation above, the critical resistance can also be calculated to avoid overheating the chip too much:

$$R_c = R_0 (1 + (0.034 / ^\circ k) (100^\circ C - 20^\circ C))$$

By multiplying the critical resistance with the current being tested, it would provide the voltage levels to stay below. After testing the wires with various widths of small current pulses, the amount of current can be increased.

Since the maximum width of pulses that can be tested with the current triggering system is 500 ms, the heating effect may not be apparent unless the amount of current is high. Therefore in addition to just using pulses, constant currents have also been used to test the chip. The methodology with using a constant current is to set the oscilloscope to a scale of seconds and triggering the signal on the rising edge of the micro wire voltage drop (channel 3). Usually for the constant current method, if the triggering and time scales are adjust properly, the LDC500 current source will disable automatically shortly after triggering. This is because the resistance of the micro wire is increasing over time which results in an increasing voltage drop across the wire. Although this is not listed in the LDC500's specification sheet, whenever the voltage drop reaches about 6.5 V to 7.0 V, the LDC500 makes a sharp beep and turns on the open circuit warning light and disables itself. The constant current method is not recommended to try at the beginning before the impulses are tested because it has been observed to permanently increase the resistance of the micro wires. This is probably due to the chromium diffusion into the gold from the bonding layer. At high temperatures, the chromium which was originally lying below the gold layer may have diffused into the gold. The electrical resistivity of gold is 24.4 nΩ•m whereas the electrical resistivity of chromium is 125 nΩ•m. The project sponsor has mentioned that this similar observation has been shown in papers he has read. [12]

As a summary, the general testing approach is outlined below:

1. Start with short pulses of 50 μs and low current of 5 mA, to observe the electrical responses
2. Increase the pulse width by 10 and collect the data until pulse widths of 500 ms
3. Increase the amount of current, with appropriate pulse widths (needs to be long enough to observe a ramping after the electrical effect comes to equilibrium)
4. If heating is not observed with the pulses, use constant currents. Start with low currents and increase the current until the LDC500 Beeps almost immediately
5. Check Resistance value of micro wire with multimeter as it may have permanently increased

5.5 Data + Analysis

Following the general testing approaches as outlined in the previous section, the IV characterization experiment was conducted on Chip 2 and Chip 3. Chip 1 was the first prototype chip produced and the micro wires were not etched very well. There are also shorts observed with the wires on Chip 1, so there is no I-V data collected for Chip 1 at all. In this section, the notable observations for Chip 2 and Chip 3 during the data collection process of the IV relationship will be described. The data collected and the data analysis will also be discussed in this section.

5.5.1 IV Data Collection

The data can be downloaded onto a computer using the oscilloscope software. The data is in the form of the voltage and time values for each of the oscilloscope channels, and the screen image. This section will provide details on the data that was collected.

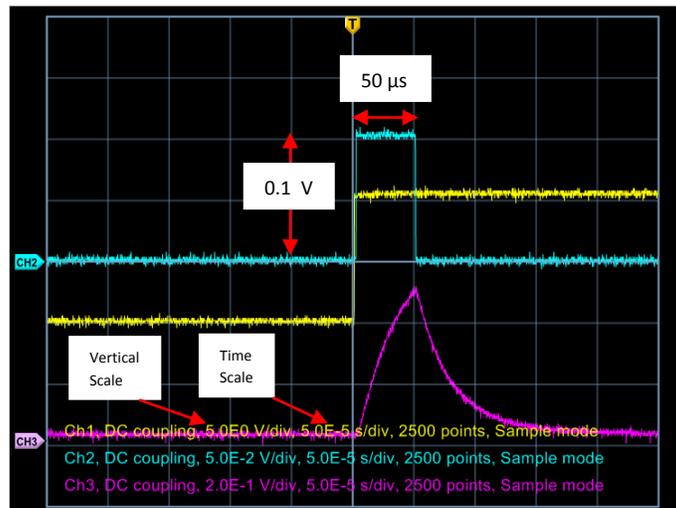


Figure 5.17: Response of a 50 μs short pulse

When a short pulse is passed through the micro wire of the chip and the current is not very high, the electrical response can be observed in the figure above. It is the data from a pulse current with a width of 50 μs . The yellow signal (Ch 1) is the signal from the Bk Precision function generator and the blue signal (Ch 2) is the signal from the F33 function generator.

Channel 2's signal has a peak to peak voltage of 0.1 V. Given a sensitivity of 50 mA / V from the LDC 500, 5 mA is being passed into the micro wire. The purple signal (Ch 3) is the voltage drop across the micro wire. The exponential ramping on the rise is suggesting that the wire is accumulating charge, and the fall is suggesting that once the current source has stopped, the accumulated charge will discharge. The figure shows that the pulse is too short and the accumulating charge has yet to reach equilibrium.

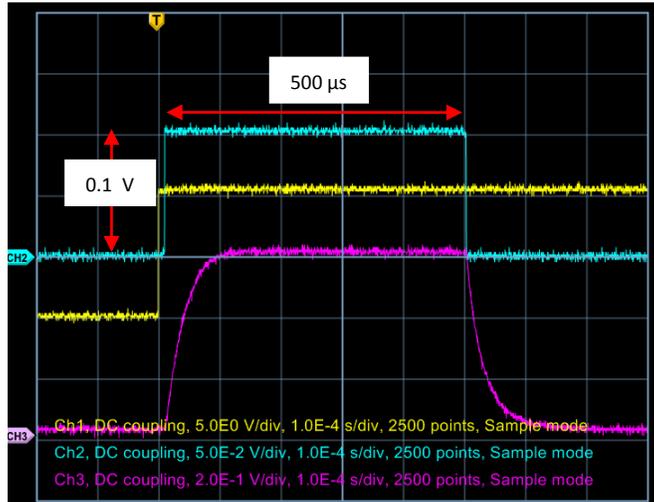


Figure 5.18: Response of a 500 μ s pulse

By looking at the 500 μ s long pulse, it can be seen that the electrical rise / fall comes to equilibrium after roughly 100 μ s for this wire. In the middle region, the voltage level is constant because there is almost no heating for such a small input current of 5 mA. The resistance determined in this region is the 4 point contact resistance over time. It can be calculated from dividing the voltage by the constant current input, 5 mA in this case. This resistance can be compared to the resistance value measured with the 2 point contact.

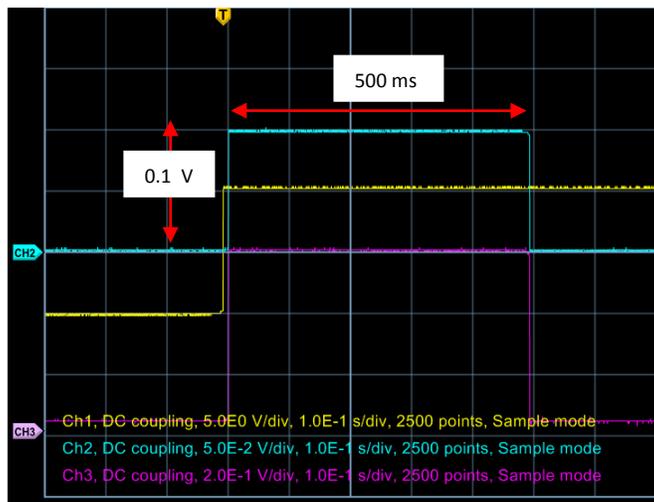


Figure 5.19: Response of a 500 ms pulse

The 500 ms response is essentially the same as the 500 μ s response except the middle region is much longer. By zooming in at the start and the end of the response, the similar electrical response can be observed. For the data analysis, the 500 ms width input's start and end electrical responses are compared to that of the electrical response at 500 μ s. Notice that the time scale for the figures below is 25 μ s per division while the time scale for the response of the 500 μ s pulse above is 100 μ s per division. After performing the data analysis (next section), it is noted that having a consistent time scale for comparing this electrical response would have made the analysis easier.

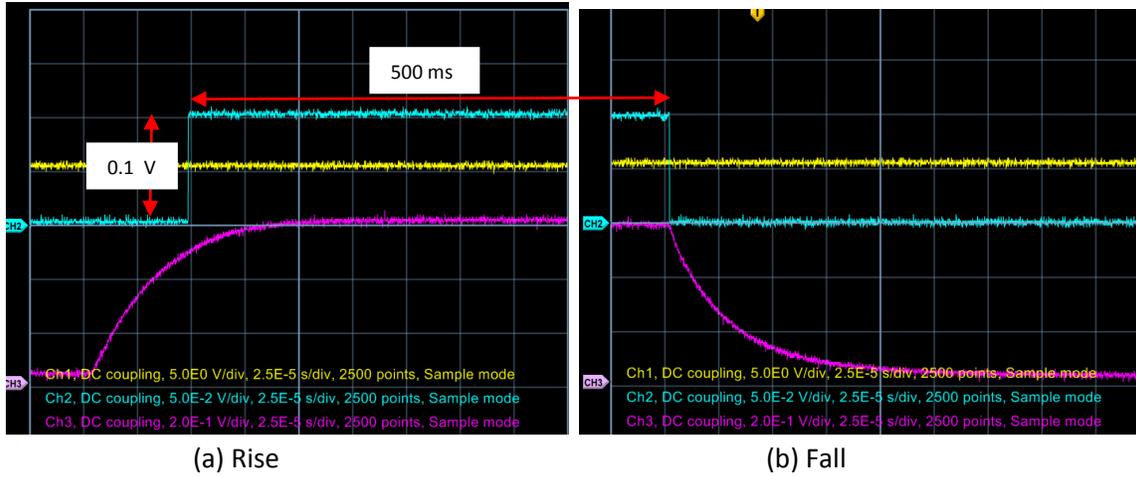


Figure 5.20: Rise and Fall response of a 500 ms pulse

The responses shown so far have not displayed any signs of heating. Now looking at the higher current responses for short intervals, there is also no heating observed.

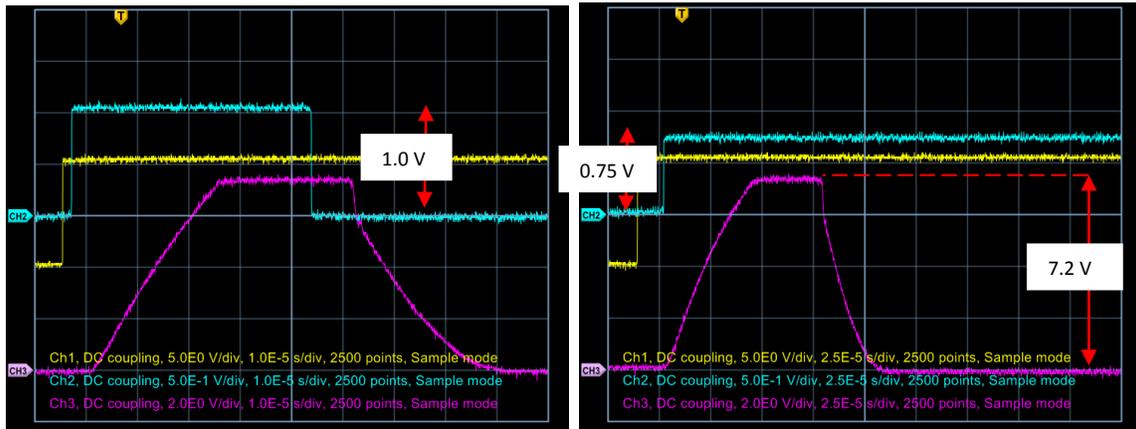


Figure 5.21: High Current Short pulses Clip due to LDC500's Voltage Limit

The two figures immediately above are measured on the chip 3's 10 μ m wire. The image on the left was powered by a current of 50 mA for 10 μ s, while the image on the right was powered by a current of 37.5 mA for 25 μ s. Since the pulse width is on the order of μ s, the wires didn't have enough time to heat up. These responses are resulted from the LDC500's limit of 6.5 to 7 V. As the high current is passing through the micro wire, the resistance is increased very rapidly until

the voltage drop across the wire reaches 7 V. At this point, the LDC500 disables itself after 35 μ s and the voltage response comes back down.

In order to observe the heating characteristics of the wires, two necessary conditions have to be met: high current and long pulse width. The following figure demonstrates the heating phenomenon of the wire.

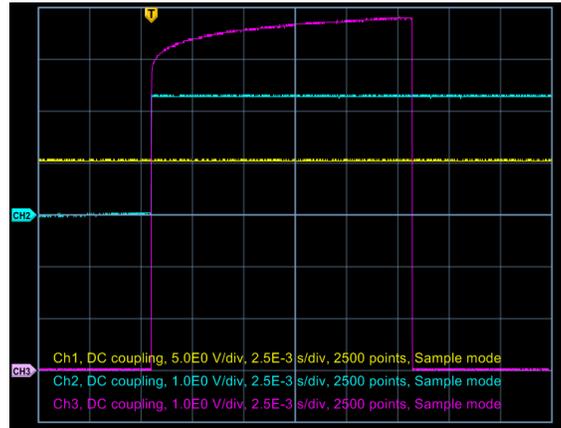


Figure 5.22: Heating Effect

The images is from the 50 μ m wire being powered at 115 mA for 12.5 ms. As the voltage drop increases with time, it means that the resistance of the wire is increasing accordingly because current is held at a constant level.

5.5.2 IV Data Analysis

The analysis shown here is the time constant analysis for the electrical response seen at the start and end of the electrical voltage response mentioned in the above section. The data for Chip 3's 10 μ m wire was measured and the analysis is described below.

Since the sampling frequency of the oscilloscope is high (60 MHz), the signal recorded is not very stable. An enlarged image of the plot from the original data shows that the signal is fluctuating. In order to smooth out the data, a filtering algorithm is developed to discard any data that causes this pattern. Knowing that the function should be either monotonically increasing or decreasing, each data point is compared with the one after it. If an anti-monotonic pattern is detected, the program would smooth it out by substituting the current data point with the previous data point. Once the data is smoothed out, it is ready for fitting. The example below is the data from the 10 μ m wire taken at with an input pulse width of 500 ms. The plot of the falling edge of the original signal is compared with the edited signal and they are shown below.

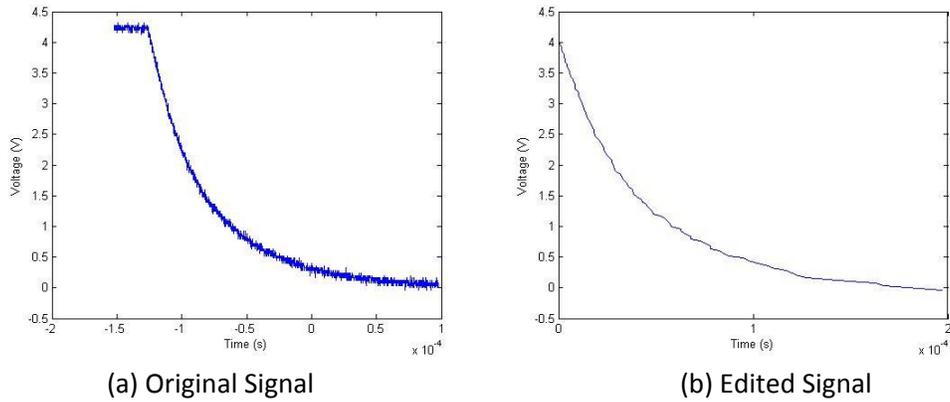


Figure 5.23: Smoothing out the falling edge signal

The time scale is on the order of microseconds. Since a linear fit is easier and more accurate than an exponential fit, the natural log is applied to the voltage values for a linear relationship.

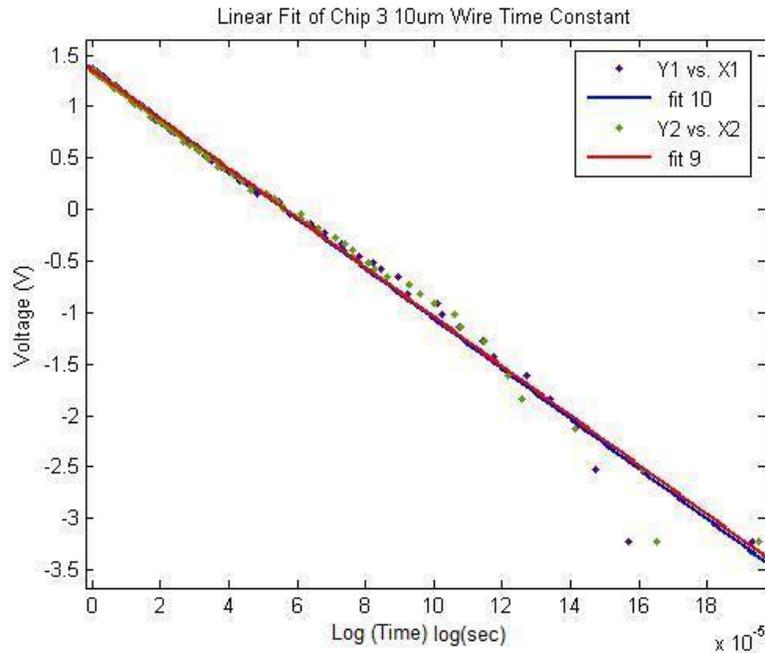


Figure 5.24: Linear Fit of Chip 3 10µm wire – Time Constant

The blue fit line is fitting the falling edge data from the 500 ms wide input pulse whereas the red fit line is fitting the falling edge data from the 500 µs wide input pulse.

Linear model Poly1: (fit 10 Pulse Width 500 ms)	Goodness of fit:
$f(x) = p1*x + p2$	SSE: 0.9016
Coefficients (with 95% confidence bounds):	R-square: 0.9903
$p1 = -2.433e+004$ (-2.484e+004, -2.383e+004)	Adjusted R-square: 0.9902
$p2 = 1.365$ (1.335, 1.395)	RMSE: 0.1007

Linear model Poly1: (fit 9 Pulse Width 500 μ s)	Goodness of fit:
$f(x) = p1*x + p2$	SSE: 0.5952
Coefficients (with 95% confidence bounds):	R-square: 0.9933
$p1 = -2.401e+004$ (-2.444e+004, -2.358e+004)	Adjusted R-square: 0.9932
$p2 = 1.353$ (1.327, 1.379)	RMSE: 0.08418

According to the fit perimeter, the time constant is $\frac{1}{p2}$.

This time constant is then used to fit the exponential rise portion of the signal. This is to check the time constant from the falling edge is actually the same as the time constant from the rising edge. The result of the check is shown below.

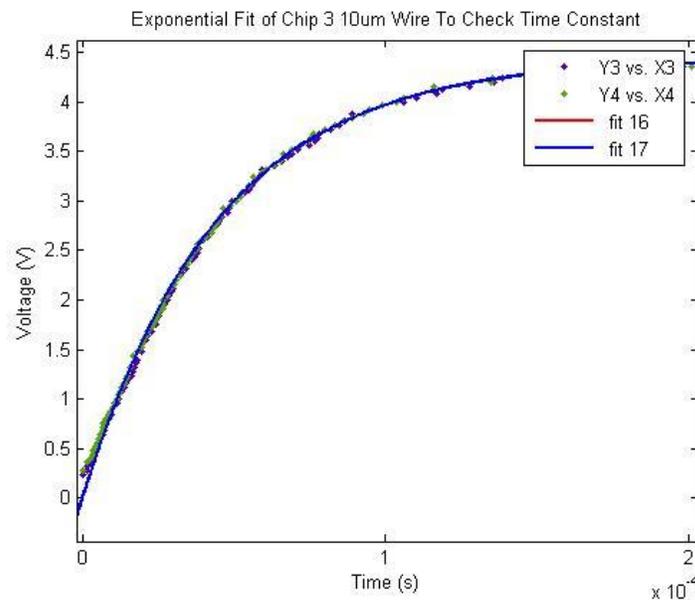


Figure 5.25: Rising Edge Fit using time constant calculated from the Falling Edge

General model: (fit16 Pulse Width 500 ms)	Goodness of fit:
$f(x) = a*(1-\exp(-b*x))$	SSE: 0.2681
Coefficients (with 95% confidence bounds):	R-square: 0.998
$a = 4.457$ (4.414, 4.501)	Adjusted R-square: 0.998
$b = 2.173e+004$ (2.129e+004, 2.217e+004)	RMSE: 0.05458

General model: (fit17 Pulse Width 500 μ s)	Goodness of fit:
$f(x) = a*(1-\exp(-b*x))$	SSE: 0.3301
Coefficients (with 95% confidence bounds):	R-square: 0.9974
$a = 4.44$ (4.39, 4.489)	Adjusted R-square: 0.9974
$b = 2.244e+004$ (2.193e+004, 2.296e+004)	RMSE: 0.0609

The fitting equation has only one free parameter, but the fit is very good because the R-square of 0.998 is so close to unity.

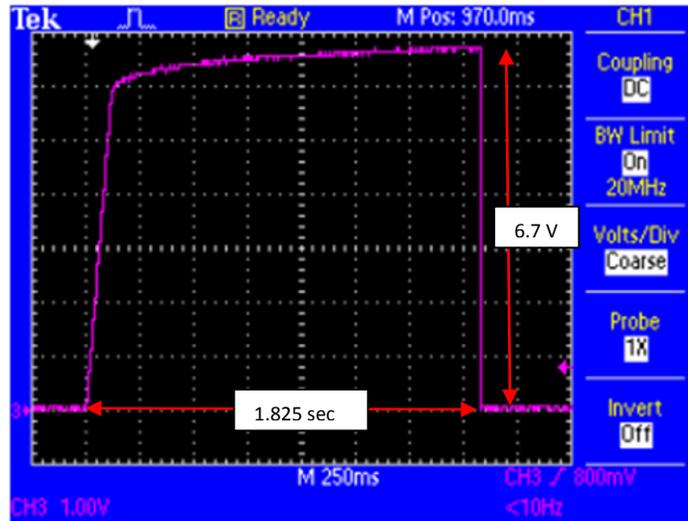
	500 ms Pulse Width	500 μ s Pulse Width
Chip 3 10 μ m Wire	4.15×10^{-5} s	4.075×10^{-5}
Chip 3 20 μ m Wire	2.99×10^{-5}	2.90×10^{-5}
Chip 3 50 μ m Wire	2.10×10^{-5}	2.005×10^{-5}

Table 7: Electrical Response Time Constants for Chip 3 wires

It was previously observed that when the test resistor is connected with the LDC500 current source, there was also a capacitance effect shown on the oscilloscope. The exponential ramping shows that the wire on the prototype chips is accumulating charge. It also points out the time it takes for the wire to come to equilibrium. The calculated time constants shown agree with the general trend that the higher resistance wires have higher time constant because the time constant is equal to RC. By assuming that the capacitance remains relatively constant for a wire under the temperature change, narrower wires will have larger resistance and thus larger time constant.

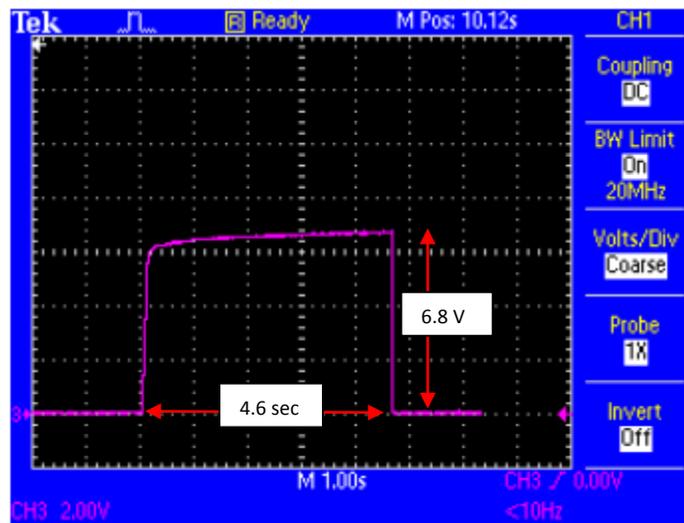
5.5.3 IV Data Discussion

During the preliminary testing in the Mina lab, a 100 mA constant current was used to observe the heating effect on the 100 μ m wire. It was observed that the heating rate or the rate at which the resistance increased over time was slow. This similar trend is observed when a constant current was used from the LDC500 on the 100 μ m wire. Using a 2 point resistance measurement, this wire is 28 Ω . The constant current knob on the LDC500 is turned until the LDC500 beeps and disables. This current turns out to be 140 mA and the signal lasted 2 seconds as shown in the figure below. The time scale is 250 ms per division and there are 7.3 divisions which yields 1.825 seconds. The 2nd graph is by restarting the LDC500 and lowering the current input slightly which is 130 mA. This new response lasts for 4.6 seconds.



TDS 2004 - 8:36:45 AM 12/23/2008

Figure 5.26: Constant Current 140 mA Input, on Chip 2 100 μ m Wire



TDS 2004 - 8:45:19 AM 12/23/2008

Figure 5.27: Constant Current 130 mA Input, on Chip 2 100 μ m Wire

When a 120 mA input was used, the signal lasted a very long time; over 10 seconds. It suggests that the higher the current is, the faster the heating is, which leads to the LDC500 reaching its voltage limit in a shorter time. For a 100 mA input, the heating would be very slow. This consistent with the result from Mina because at Mina, the equipment was limited at 100 mA, and the rate of increase for resistance was very low.

For the heating characteristics, from theory, as current runs through a wire, heat is generated. Due to the poor conduction of heat, the temperature of the wire will increase exponentially over time. The chip may fail from the heat. However, for the data where the input pulse does not have a high current, it appears that there is some equilibrium temperature that

the wire reaches. For the same amount of current, this equilibrium temperature (voltage drop) seems to be about the same for the various lengths of pulses when just looking at the oscilloscope screen.

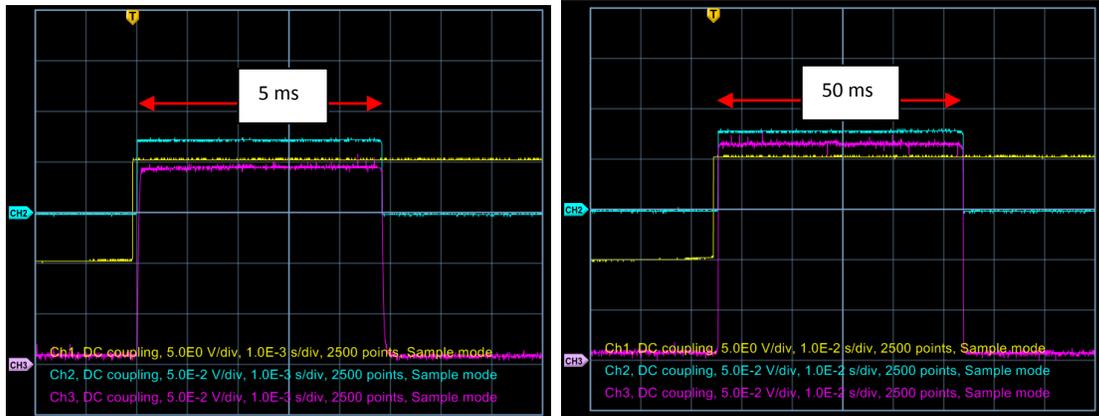


Figure 5.28: Low Current Input, Equilibrium Voltage Drop / Temperature

The above images are downloaded from the oscilloscope screen. The left image is generated when testing the Chip 2 50 μm wire with a 3.75 mA current with a pulse width of 5 ms. The right image is generated when testing the same 50 μm wire with a 3.75 mA current of with a pulse width of 50 ms. Each pulse remains constant comparing with other pulses. But, when the graphs are cross-compared with each other, the resistance is found to have increased for the pulses with longer width. The resistance of all three wires on chip 3 under different pulse width is calculated by Matlab and the result is shown below.

	500 ms Pulse	50 ms Pulse	5 ms Pulse	DMM Value
Chip 3 6 μm	342.64 Ω	337.77 Ω	318.56 Ω	315.3 Ω
Chip 3 20 μm	122.13 Ω	122.01 Ω	121.61 Ω	114.2 Ω
Chip 3 50 μm	58.07 Ω	55.316 Ω	52.567 Ω	51.2 Ω

Table 8: Resistance of Chip 3 Wires under different Pulse Width

Assuming that the resistance measured from the DMM are the resistance at 20°C, the temperature of each resistor powered by different pulse width is listed below.

	500 ms Pulse	50 ms Pulse	5 ms Pulse
Chip 3 6 μm	25.50325554°C	20.96042984 °C	3.040988041 °C
Chip 3 20 μm	20.42340579 °C	20.11435047 °C	19.08416607 °C
Chip 3 50 μm	39.46461397 °C	23.64430147 °C	7.852711397 °C

Table 9: Temperature of Chip 3 Wires under different Pulse Width

The temperature rising rate slows down exponentially as the pulse length increases.

For the heating effect Figure 5.20 above, the 50 μm wire is running at a current of 115 mA. The output pulse (Ch 3) from the wire is much shorter than the triggering pulse from the function generator. This indicates that the voltage reached the limit of the equipment and is therefore turned off. The voltage rise can be converted to temperature rise according to equation 2 in the technical background. Since the temperature rise demonstrates an exponential relationship with time, a time constant can be found by fitting an equation transformed by equation 5.

$$T = T_0 + a(1 - e^{-\frac{t}{\tau}})$$

Equation 9: Transformed Equation of Temperature difference between Wire and Substrate

Where “a” and “τ” are free parameters in the equation. By taking the natural log of time the relationship becomes linear. The τ value can be calculated as following:

$$\tau = \frac{(p_2 - T_0)}{p_1}$$

Equation 10: Heating Time Constant

The results of the fits are provided below. For the second fit, although the first few data points are not in a line, the most important data are the ones in the end because the natural log was taken above. The discrepancy in the linearity is actually just on a small region.

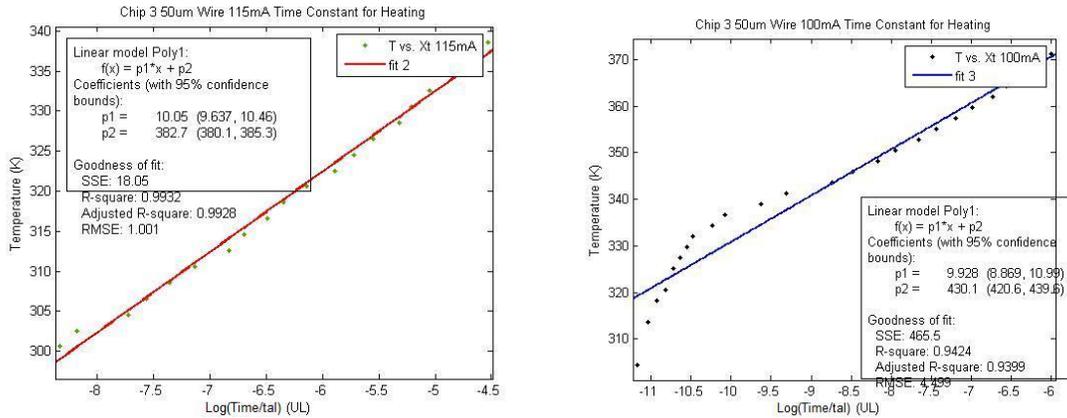


Figure 5.29: Time Constant of Heating

The heating constant was calculated for the 100 mA input pulse and the 115 mA input pulse. The time constant for the 100 mA pulse is larger than the value of the 115 mA pulse. This is because higher current wire heats up faster and it takes less time (lower time constant) to reach the equilibrium temperature. This value agrees with the observation

	100 mA 2.5 ms	115 mA 10 ms
Chip 3	13.809 ms	8.9254 ms

6.0 Conclusions

The objective of this project is to compare the actual width measured and the desired width of each wire on the chip, observe the surface topological details of the chip, and to measure the I-V characteristics of the wires with four point measurement technique. In general, the objectives of this project are met.

The data from the SEM and the White Light Interferometer shows that the actual width of the wires is very close to the desired value. Although one of the wires differ from the desired width by 35 to 40%, most wires are 4% to 7% less than the desired width. The slope of the linear fit on five of the data points approaches unity which indicates that the incremental width calibrations are well adjusted; the actual width of the wire increases correspondingly with a 1 to 1 ratio. Thus, knowing the desired width of the wires and the percent error of the width of the actual wire, the error can be compensated by increasing the programmed width by 4% to 7%.

According to the analysis on the SEM images, it can be seen that the smoothness of the edge is directly related to the output power of the laser. The standard deviation from two sets of wires indicates that high laser power produces rusty edges, while low laser power produces smooth edges. In addition, according to images from the White Light Interferometer, high laser power may damage the substrate underneath the gold layer.

Although the Profilometer is incapable of measuring the width or the depth of the cut, it does provide valuable information about the edges of the cut. From the plot, the edge tilts a few nm upward due to high temperature ablation from the laser. This phenomenon is also observed by the data from the White Light Interferometer. This further strengthens the importance of carefully controlling the power level of the laser.

A testing bench that uses four point measurement technique was constructed. It connects to a current source and an oscilloscope to take data. From the oscilloscope images, it is shown that each wire requires time to charge up and discharge. Therefore, each wire acts as if there is a capacitor connected in series with the resistor. The time constant value for each wire on chip 3 is deduced by fitting the discharging (falling) part of the signal, and the value is then confirmed by fitting the charging (rising) part of the signal. The time constant is on the scale of 20 μs and the value increases with increasing resistance. These quantities agree with the trend stated in the theory.

Based on the I-V data, the heating of the wires can be observed as the voltage response of the wire increases with time. However, the voltage does not increase exponentially as described in a paper. There appears to be an equilibrium temperature for different pulse widths and strength. For high current pulses, the heating curve is very steep and the current source would turn off immediately before it reaches equilibrium. But for low current pulses, there is enough time for the wire to reach equilibrium temperature and the voltage will remain constant throughout the measurement. Analyzed in Matlab, it was found that the time constant of heating is on the scale of milliseconds, and the magnitude of this constant is inversely proportional with the input current.

When measuring the heating characteristics of the wires on the second prototype chip, constant current with high magnitude was used and the wire was kept at a few hundred degrees for a long time. After the measurement, the resistance of the wire almost doubled and would never return to the original value. This is because the adhesive layer of chromium between the gold and the SiO_2 has diffused into the gold as the temperature was kept high. In addition, this phenomenon can also explain why the resistance of the wires are larger than the calculated resistances based on the properties of gold. During the manufacturing process, the instantaneous laser ablation process of the gold may have heated up the small region to extremely high temperatures causing the diffusion of chromium.

7.0 Recommendations

Scanning Electron Microscope

When using the SEM, it is recommended to use the primary detector to collect the signal for imaging. These images are easier to analyze in Matlab than the secondary detector because the contrast between black and white is very well refined. However, the secondary detector does pick up more information on the images.

By taking the medium sized (resolution, file size wise) SEM pictures, in addition to the high resolution images, the length scale of the image can be imprinted onto the image.

The depth of the wire ablation cut can be measured if the chip is cut in half. The cross section of the chip can be examined by the SEM for depth information. Knowing the depths of the cut and comparing it with the thickness value of the gold layer, it becomes possible to see whether the laser has cut through the gold layer or not. If the depth is deeper than the thickness, the substrate could be damaged. On the other hand, if the depth is shallower than the thickness, there could be a short circuit. In addition, by viewing the cross section of the chip, information about the thickness of the chromium and magnesium fluoride layers can be obtained since the SEM has the ability to determine the composition through the rate at which the electrons scatter.

Profilometer

Since the stylus tip on the Profilometer detector has a larger diameter than the width of the cuts, it is suggested to enlarge the width of the cut on a side sample just for the purpose of observing it with the Profilometer. The Profilometer is relatively easier to use because it requires no pre-treatment on the chip like the SEM, or adjustment on the position of the platform like the White Light Interferometer.

Current - Voltage Relationships (IV)

Due to the observation that the resistances of two wires on Chip 2 doubling when they were inputted with high constant current for a long time, it is advisable to carry out the measurements with pulsed signals in the beginning to avoid permanent resistance change. Testing with high constant current should only be carried out when all the characterization data is collected and extreme condition data is expected by the sponsor.

Currently, the pin connectors that are used to make contact on the wire pads are relatively hard. This is required for surfaces that have a coating on it. Note that the gold layer is coated with MgF, and the pin has to pierce through the layer to physically touch the gold. If the pins are soft, it will elastically deform and bend away from the surface. Newly ordered samples do not have protective coating on top of it. Therefore, making new softer pins is necessary to avoid scratching the surface for future measurements.

The LDC500 current source has a limit on the voltage output. If the voltage output is above 6.5V, it will beep and disable automatically. Because of this, for wires with large

resistance, the input current will be very small. Therefore, it is very difficult to observe heating on these wires. In order to observe heating on these devices, an equipment of high voltage output limit needs be used.

Since the LDC500 current source and the oscilloscope both connect to the wire. It is possible to mix up the terminals and accidentally connect the positive terminal of the LDC500 current source to the ground of the oscilloscope causing a short circuit. If this happens, the oscilloscope will not pick up any signal. A connector box with BNC connectors can be made to link the LDC500 current source and the oscilloscope.

Appendix

Glossary

Laser ablation	is used to etch away the material on top of the substrate; this technology is used in micro-chip fabrication.
Atom Chip	is an IC that is used to run high current in it to produce magnetic field strong enough to trap an atom.
Femtosecond Laser	is a very high pulse and high energy laser that can be used to cut materials on a small scale.
Photolithography	The most popular technology used to fabricate ICs
Substrate	A semi-conductor material, usually referred to as wafer that is made from Si, or GaAs and is coated by conductive material to make ICs.
Surface Profiler	A device that can measure the surface topography on the scale of micro to nanometers.
Wire Bonder	A machine that is used to attach wires on the surface of an IC

Abbreviation

UBC	University of British Columbia
QDG	Quantum Degenerate Gases
MiNa	Microsystems and Nanotechnology Group
AMPEL	Advanced Materials Processing Engineering Laboratory
MEMS	Micro Electro Mechanical Systems
DMM	Digital Multimeter
SEM	Scanning Electron Microscope
ENPH	Engineering Physics
AFM	Atom Force Microscope
PCB	Printed Circuit Board
BOM	Bill of Materials
IV	Current - Voltage
FS	Femtosecond Laser
SHCS	Socket Head Cap Screw
Si	Silicon
SiO ₂	Silicon Dioxide
Al	Aluminum
Au	Gold
Cu	Copper
Cr	Chromium

Sn	Tin
μs	microsecond
nm	nanometer
μm	micrometer
cm	centimeter
mm	millimeter

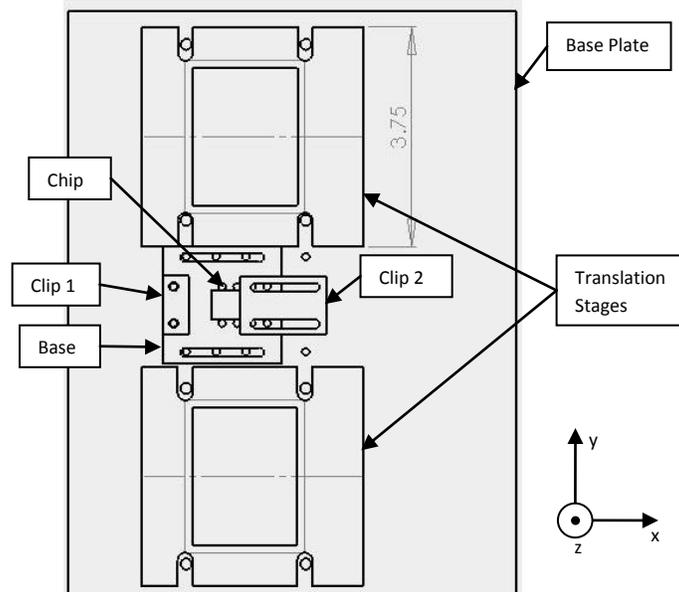
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Barsch, N. (Laser Zentrum Hannover e.V.); Korber, K.; Ostendorf, A.; Tonshoff, K.H.

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http://uwspace.uwaterloo.ca/bitstream/10012/3374/1/thesis_orcherry.pdf

A. Wire Alignment / Connections Instructions for Testing Apparatus



Note: Micrometers on translations follow the left hand rule for the z direction and the right hand rule for the x and y directions.

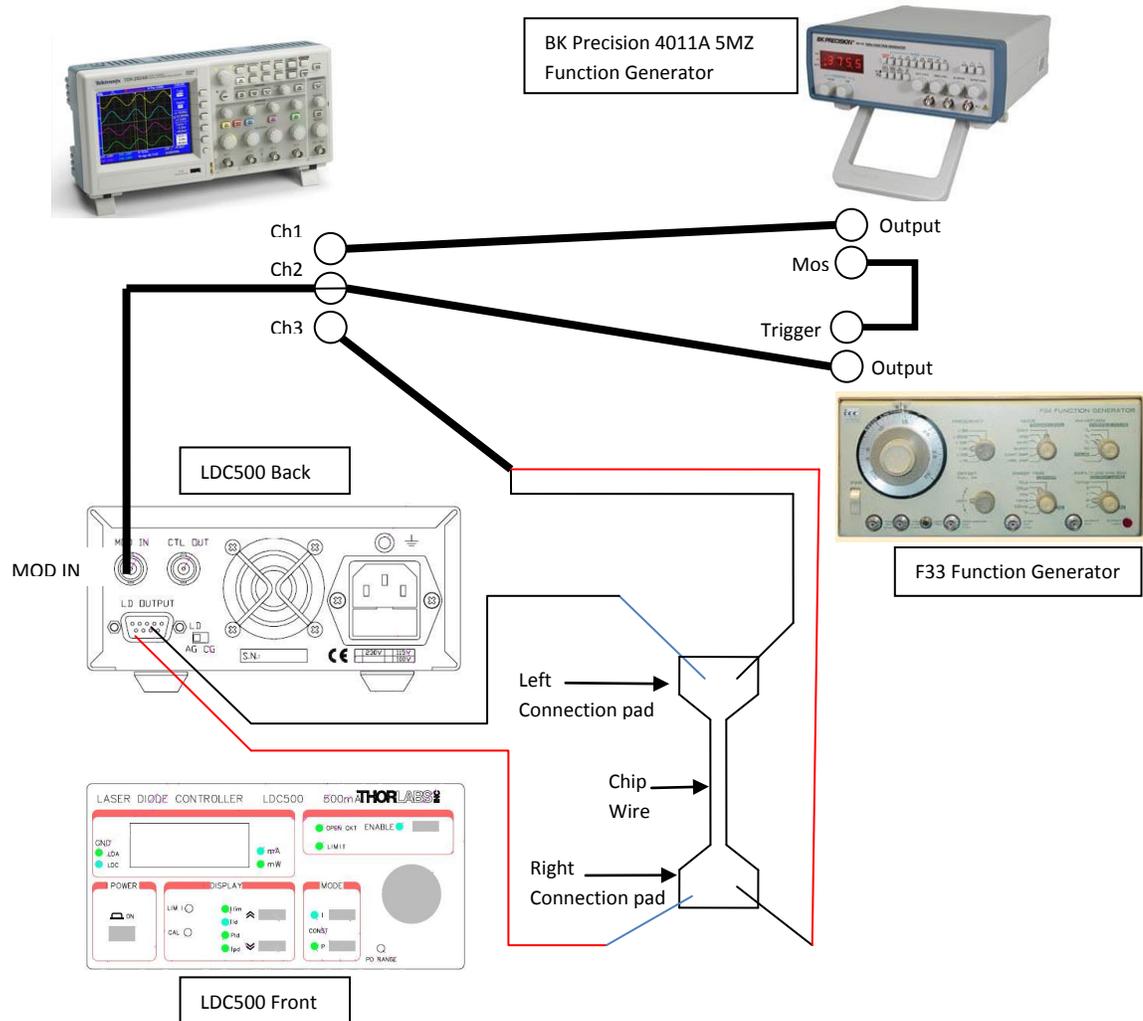
1. Make sure the two translation stages are properly stabilized on the base plate; unless necessary, they don't have to be moved at all
2. Use lab clips or other clamps to hold the base plate down on a clean working table
3. Lift the test probes (+z) and translate them away from the center testing area (-y from bottom, +y for top, and -x)
4. Loosen the top four screws on clip 2, and move it outward (+x).
5. Use tweezers to remove the prototype chip that is there.
6. Use tweezers to take another sample out of the case and carefully place it on the testing base.
7. Stabilize the four screws on clip 2 to hold on to the new sample.

Note: Since the translation stage can only move limited distances of 3 mm, the wire has to be located as close to the pin as possible

8. Loosen the four screws that hold the testing base so that it can slide back and forth (x).
9. Identify the wire to be tested and then move the testing base (x) so that the wire is closely underneath the pin connectors
10. Stable the four screws on the testing base
11. Adjust the x-y position knob first so that the two pin connectors are on the boarder of the pad.
12. Carefully lower down the connectors with the z-axis knob.

13. Before the pins touch the gold surface, switch to the finer tuning knob to lower down the pins to avoid scratching the surface.
14. Have one pin touch the inside of the pad and the other touch the outside of the pad.
15. Have a digital multimeter (DMM) ready and connect it with the two pins on one side of connector.
16. Measure the resistance. If the resistance is small, that means the wire is not properly cut and is shorted with the area outside the laser cut. If the resistance is high or infinity, that means there is no contact and the wire is a good wire.
17. If the wire is good, lift up the two pins and move them back above the pad with the x-y axis knob.
18. Lower down the two pins (-z)
19. Check the resistance with the DMM, it should be around 1Ω
20. Repeat step 11 – 20 for the second translation stage
21. Check the resistance across the wire
22. Connect the one white wire on each side with the LDC500 current source.
23. Connect the other wire on each side with the Oscilloscope. Be careful of the color schemes of the wire. The red wire from the LDC500 is positive while the black wire is ground. The red wire from the BNC connector is positive while the black wire is ground. The wires that are connected on one side of the pins should be all red while the other side should be all black to avoid a short circuit.

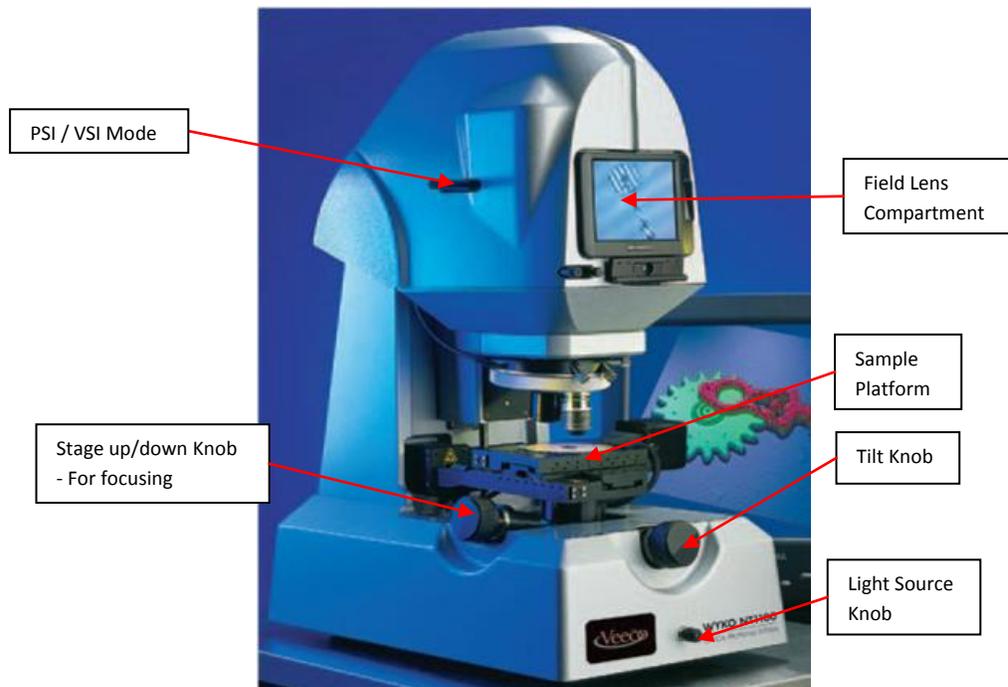
B. IV Testing Protocol



- Connect the equipments as shown
- Turn on the Bk Precision function generator.
- Use a frequency of 5Hz to start with, and increase the frequency afterward, and use square waves
- Turn on the secondary triggering function generator and select external trigger as the triggering method.
- Use a pulsing frequency of 1 kHz, a square waveform, and a low voltage of 0.1 V to start with and increase the value slowly afterward.
- Make sure the secondary triggering device is connected with the LDC500 current source. Otherwise, the current output will be constant.
- Make sure the offset (current knob) on the LDC500 is set to zero.

- Check the current limit of the current source and make sure that it is high enough to output required current
- The oscilloscope trigger should be set on channel one, the triggering mode should be set to normal and on the rising edge of the pulse.
- The time scale should be adjusted according to the triggering device's frequency so that one full cycle of the signal can be seen on the screen.
- The voltage division should be adjusted property to use the screen of the oscilloscope fully.
- If there is no signal initially, one could use the button labeled "auto" to find where the signal is. Then the settings can be adjusted for a better vision
- Begin testing by following the general testing approach as outlined in section 5.4.2
 1. Start with short pulses of 50 μ s and low current of 5 mA, to observe the electrical responses
 2. Increase the pulse width by 10 and collect the data until pulse widths of 500 ms
 3. Increase the amount of current, with appropriate pulse widths (needs to be long enough to observe a ramping after the electrical effect comes to equilibrium)
 4. If heating is not observed with the pulses, use constant currents. Start with low currents and increase the current until the LDC500 Beeps almost immediately
 5. Check Resistance value of micro wire with multimeter as it may have permanently increased

C. White Light Interferometer Measurement Instructions



Notes:

- A reflective surface is required on the sample surface
- There are two lens:
 - Objective Lens commonly 5 x
 - Field Lens commonly 0.5 x
Magnification 2.5 x
- There are two modes:
 - PSI Mode – Precise, Smooth
 - Make sure the light does not saturate in PSI
 - VSI Mode – Longer range

Procedures:

1. Open the Field Lens Compartment and check the lenses used in the device. Estimate if it is sufficient to see the patterns of a certain scales.
2. Change the field lens if necessary
 - slide in the new Field Lens, and close the compartment
3. Lower down the testing platform
4. Take out the sample with tweezers and carefully place it on the testing platform
5. Turn on the equipment and open the software (Vision)
 - Turn up the light source (make sure this light is off when finished)

6. The left screen has all the buttons to control the device while the right screen shows the image of the White Light Interferometer
7. Enter the corresponding lens in the settings
8. The intensity of the light should be set low in the beginning to avoid any red color on the right screen. If the intensity is high, the White Light Interferometer could be damaged.
9. The platform is then slowly lifted until an interference fringe pattern can be seen on the right screen.
10. The platform can be tilted to have either pure black or pure white (one fringe) to cover the entire screen.
11. Once the image of the White Light Interferometer (Right Screen) is covered with a monotonic color, the measurement can be made by pressing new in the software interface
 - Some useful Analysis Options are:
 - Tilt removal
 - Filtering
 - Mask Points

D. SEM Testing Protocol

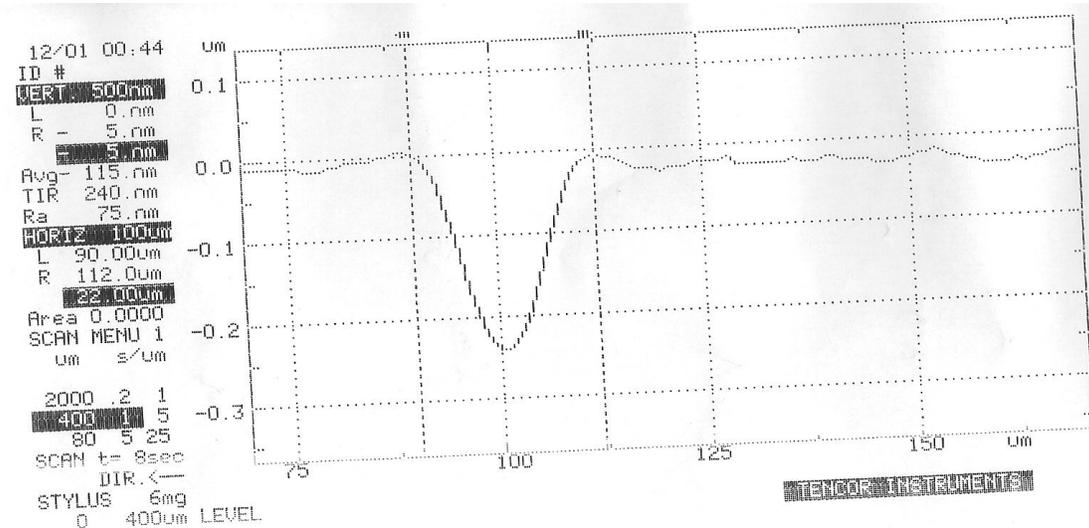
An existing SEM instruction manual can be found next to the SEM machine in Room 45 basement of EOS. A soft copy is available upon request from Sasha Wilson (swilson@eos.ubc.ca).

E. Additional Profilometer Data

This is the Profilometer data for Chip 2 100 μm wire.

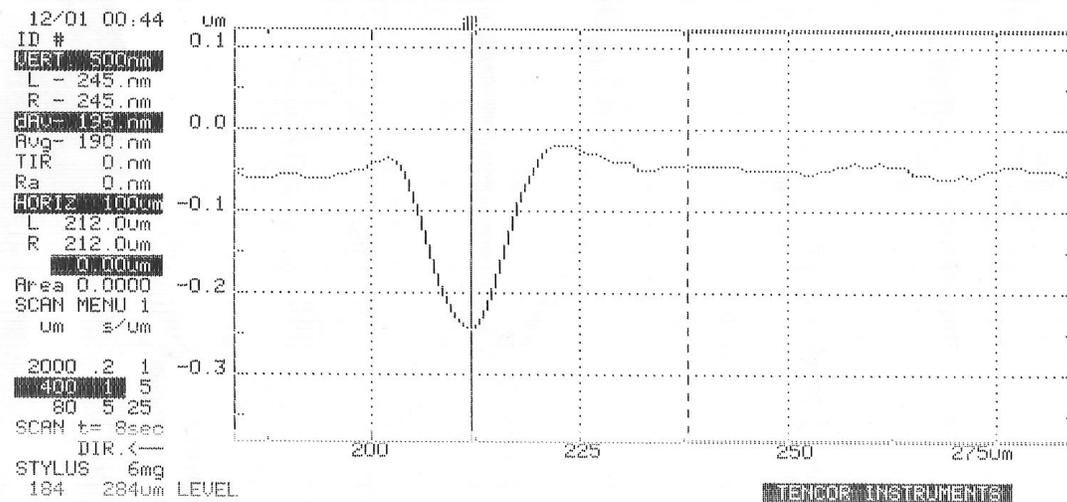
Image of the left Cut

The left cut is shown below, and similar with the right cut, the surface tilts upward at the edge of the cut indicating a deformation after the ablation. The bell shaped curve resembles the shape of the stylus tip on the Profilometer detector instead of the depth of the cut.



Depth Measurement

Although the depth information is provided below, it is unknown how different it is from the actual width. However, this gives a lower bound on the depth of the cut which may become useful for future reference. The measured depth here is 0.19um.



F. Mina Preliminary IV Testing Report

Data collection on 2008/11/7

Procedure:

Measurement on the resistances of the 100 μm and 200 μm wires of the second chip were performed in the MiNa lab with assistance from Mark Greenberg. The lab used two micrometer stands, a Keithley 2602 Multimeter and an overhead ccd camera.

In order to make contact with the gold layer, the pin has to scratch the gold surface back and forth to pierce through the protective Magnesium Fluoride layer. The scratch can be clearly seen under the probe of the camera.

The resistance measured before scratching is 34 Ω for the 200 μm wire, and 75 Ω for the 100 μm wire. After scratching the surface slightly with the probe pin, the reading shows a resistance of 28.46 Ω . The resistance is measured at several places on the connection pad to make sure a good contact has been made.

1 st measurement	28.46 Ω
2 nd measurement	28.45 Ω
3 rd measurement	28.51 Ω
4 th measurement	28.52 Ω

The resistance is measured at a constant current of 1 mA

Next, the resistance is measured under the condition of increased current. The current change can also illustrate the voltage change with respect to time.

Current (mA)	Resistance(Ω)	Current (mA)	Resistance(Ω)
5	28.44	-5	
10	28.47	-10	28.48
20	28.57	-20	28.58
30	28.73	-30	28.75
40	28.99	-40	29.00
50	29.34	-50	29.32
60	29.79	-60	29.75
70	30.32	-70	30.25
80	30.88	-80	30.85
90	31.65	-90	31.57
100	32.46	-100	32.32

Next the resistance was measured when the current is held at a constant of 100 mA. The resistance data is shown below:

Time	Resistance Ω
0s	31.9
1min	32.89
5min	33.07

Next, the wire of 200 μm was measured

Current(mA)	Resistance(Ω)	Current(mA)	Resistance(Ω)
10	15.45	-10	16.24
20	15.88	-20	16.84
30	16.07	-30	16.70
40	16.20	-40	16.77
50	16.30	-50	16.69
60	16.42	-60	16.79
70	16.54	-70	16.84
80	16.69	-80	16.95
90	16.85	-90	17.11
100	17.05	-100	17.27

Then the current was held constant at 100 mA for five minutes to collect the following data

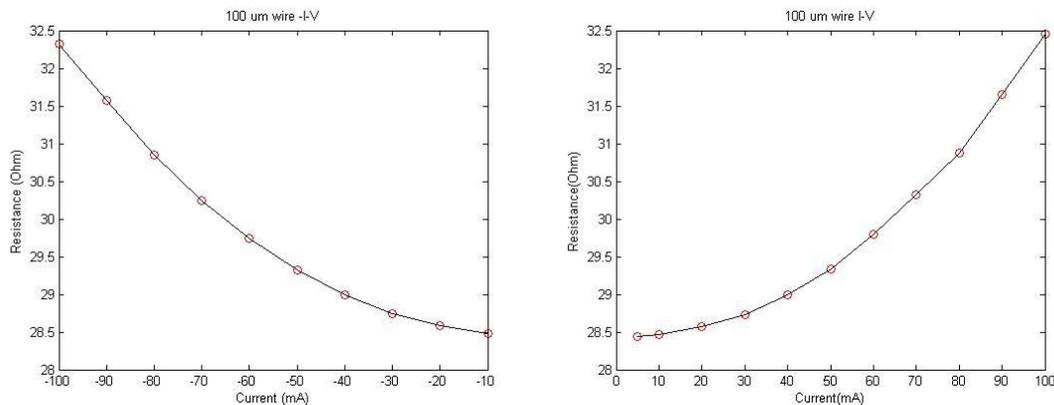
Time(s)	Resistance(Ω)
0s	16.88
1min	17.20
5min	17.21~17.22

The resistance doesn't change much during the last 4 minutes.

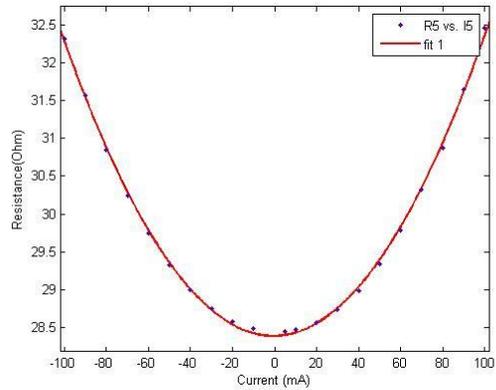
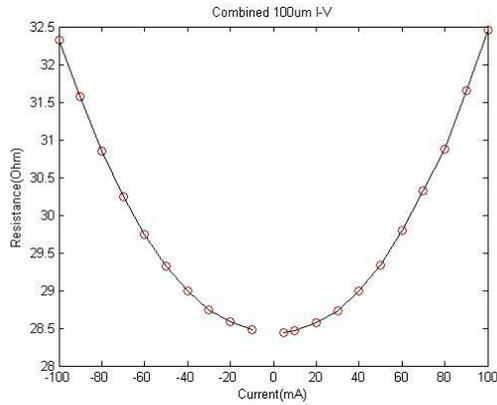
Note: Before actually collecting the data, the resistivity between the pad and the ground area was measured to make sure that the wire and the ground is properly insulated. And the resistance shows 0.5 G Ω which allows us to conclude that the wire is properly insulated.

Analysis:

The current vs. resistance curve was plotted for the 100 μm wire.



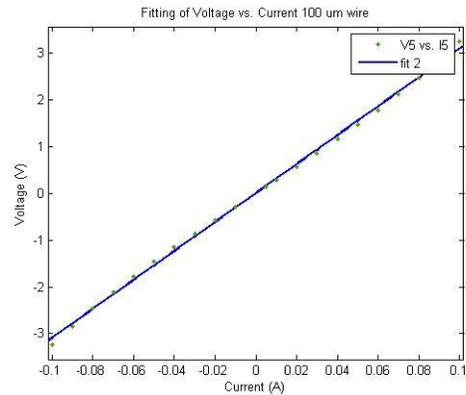
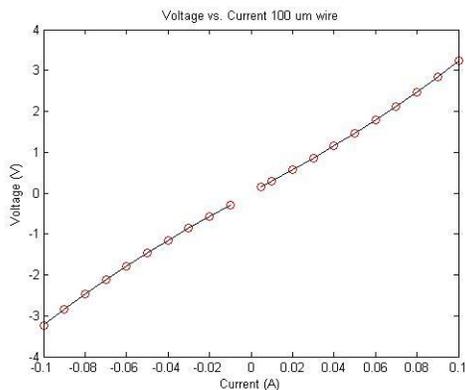
The plots demonstrate an exponential pattern. The resistance will continue to grow as the current increases. The resistance increases much faster than the current increase. The two plot above are combined into one graph below



The shape of the graph is almost parabolic. The resistance is not constant with respect to the current increase. On the other hand its relationship is fitted below.

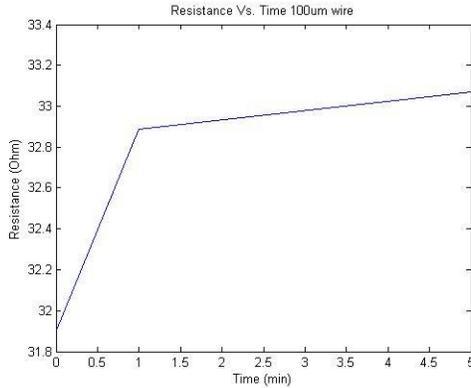
Linear model Poly2:	Goodness of fit:
$R(i) = a \cdot i^2 + b \cdot i + c$	SSE: 0.03589
Coefficients (with 95% confidence bounds):	R-square: 0.999
$a = 0.0003952$ (0.0003889, 0.0004015)	Adjusted R-square: 0.9989
$b = 0.0004003$ (6.224e-005, 0.0007383)	RMSE: 0.04465
$c = 28.38$ (28.35, 28.41)	

The voltage can be calculated by multiplying the resistance and the current, and it is plotted against the current. The two sets of data are combined to generate a plot shown below.



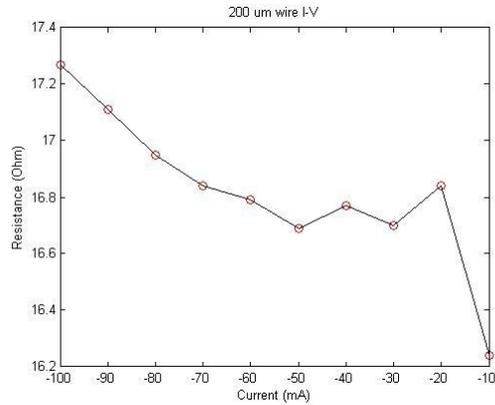
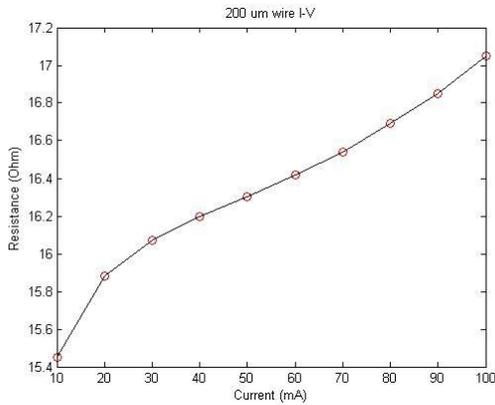
Linear model Poly1:	Goodness of fit:
$f(x) = p1 \cdot x + p2$	SSE: 0.1031
Coefficients (with 95% confidence bounds):	R-square: 0.9986
$p1 = 30.98$ (30.43, 31.54)	Adjusted R-square: 0.9985
$p2 = 0.0008515$ (-0.03279, 0.03449)	RMSE: 0.07365

The plot of the resistance vs. time is provided below.



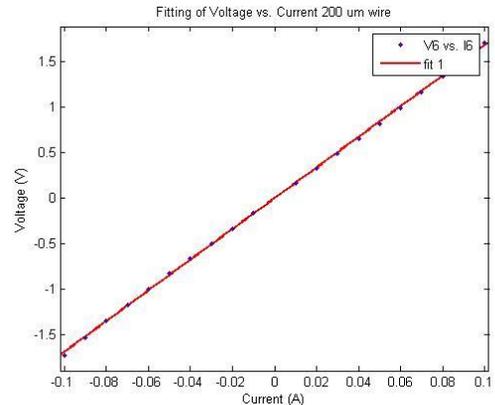
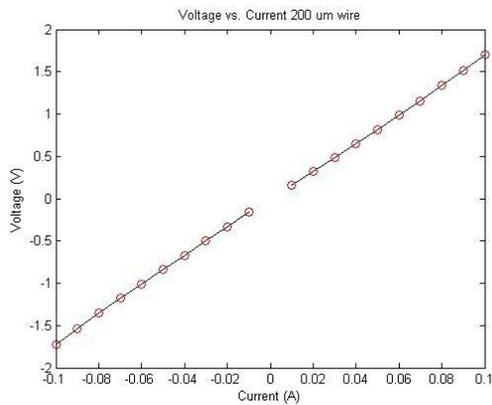
It shows that the resistance is increasing over time but at a very slow rate. The slow increase of the resistance is probably because the current input isn't too high.

The current vs. resistance curve was plotted for the 200 μm wire.



The graph plotted doesn't show a clear pattern like the 100μm wire. There is still the trend of increasing resistance.

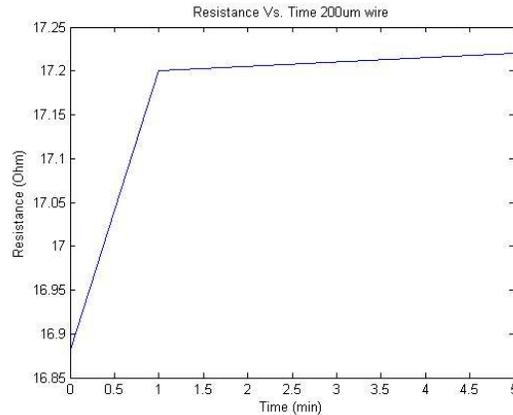
The voltage vs. current is plotted as below. It is then fitted linearly.



Linear model Poly1:	Goodness of fit:
$f(x) = p1*x + p2$	SSE: 4818
Coefficients (with 95% confidence bounds):	R-square: 0.9998
$p1 = 16.85 (16.73, 16.98)$	Adjusted R-square: 0.9998
$p2 = -9.885 (-17.57, -2.199)$	RMSE: 16.36

This shows the resistance increases uniformly with respect to the current increases.

The resistance is plotted against time.



This figure also shows that the resistance is increasing over time, but it is increasing slower than the 100 μm wire. This is expected because wider wires can handle larger currents.

Conclusion:

The data was measured without using the method of four point contact. The contact resistance is inherent in the entire measurement process. The resistance is thus higher than the theoretical value. The theoretical value of resistance is 11.7 Ω for the 100 μm wire, and 5.86 Ω for the 200 μm . The theoretical values are almost 3 times smaller than the value measured in the MiNa lab at Kaiser. This could be because of the large contact resistance between the pin and the pad. However, it must be further tested with the four point contact measurement technique for a more profound conclusion.

Also, the heat conduction and the temperature increase seem to be rather slow. It is unclear where the excess amount of heat is going such that the wire can stay at a stable temperature.

G. White Light Interferometer Data

The following data is collected from the White Light Interferometer.

Chip 1			
Cut (μm)	Width (μm)	Cut (μm)	Programmed Width (μm)
11.1669	20.0074	10.9343	20
9.5384	52.5775	10.7016	50
12.0975	9.3058	13.028	10
7.44	14.4239	7.4446	10

Chip 2			
Cut (μm)	Width (μm)	Cut (μm)	Programmed Width (μm)
13.9596	46.994	13.3	50
14.1913	93.0576	15.1219	100
15.4327	192.9084	15.4327	200

Chip 3			
Cut (μm)	Width (μm)	Cut (μm)	Programmed Width (μm)
13.0281	46.9941	13.4933	50
12.7954	19.0768	11.3996	20
14.8892	6.0487	14.4239	10

Below are the plots of the programmed width against the actual measured width. The plot is generate with Matlab.

Data of the first plot

Actual Width Y-axis (μm)	Programmed Width X-axis (μm)
20.0074	20
52.5775	50
9.3058	10
14.4239	10

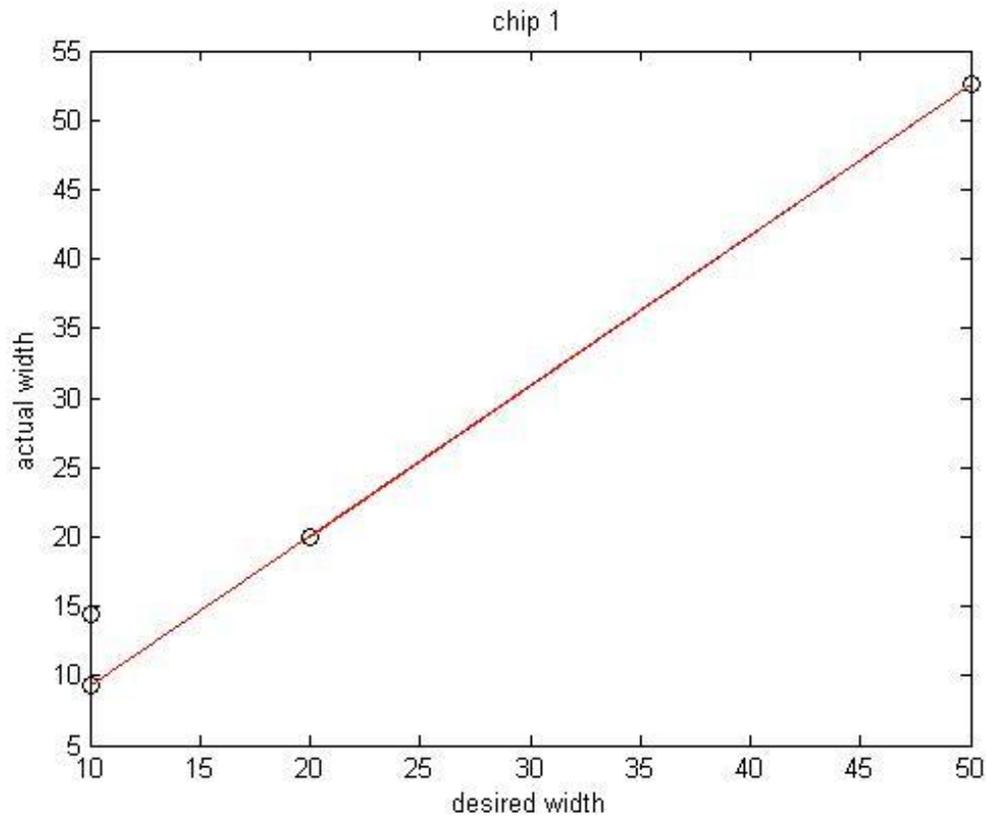


Figure 2

The matlab code to generate this plot is shown below:

```
x1 = [20,50,10,10];  
y1 = [20.0074,52.5775,9.3058,14.4239];  
figure(1); plot(x1,y1,'ko', x1,y1,'r-');  
xlabel('desired width');  
ylabel('actual width');  
title('chip 1');
```

The first chip has four sets of wires and two of them are the same width, 10 μm . Therefore, the plot has two data points whose x-axis value shows 10 μm but with different actual width.

Data of the second plot

Actual Width Y-axis(μm)	Programmed Width X-axis (μm)
46.994	50
93.0576	100
192.9084	200

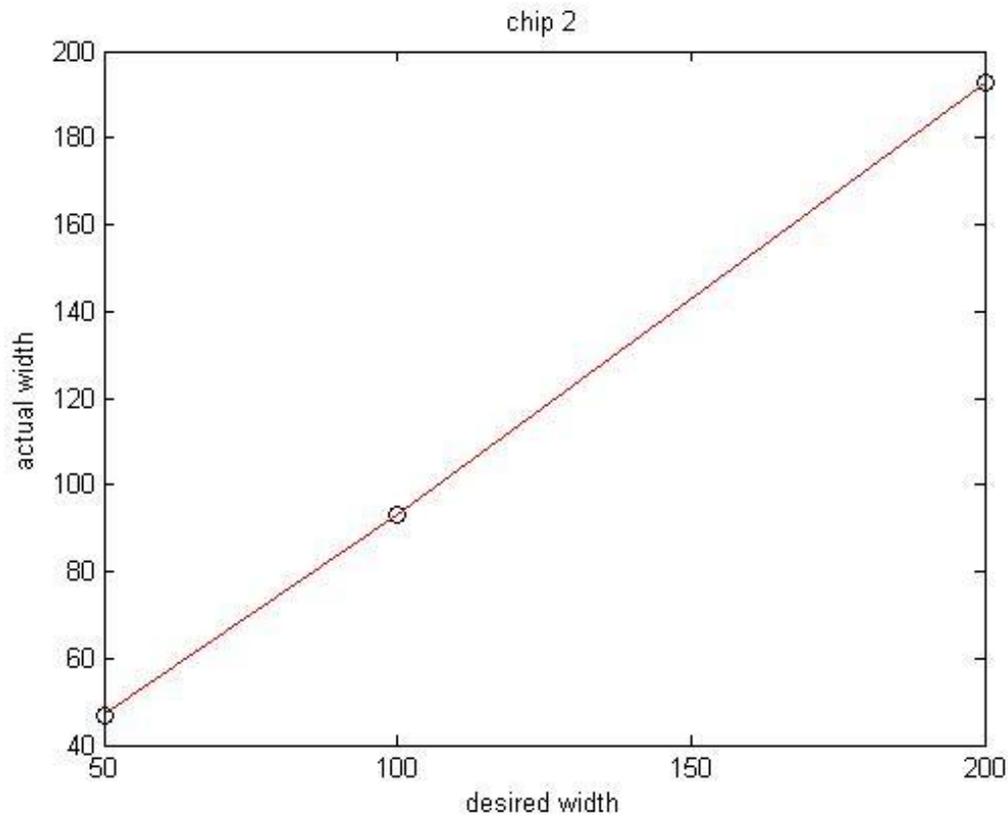


Figure 3

The matlab code to generate this plot is shown below:

```
x2=[50,100,200];  
y2=[46.994,93.0576,192.9084];  
figure(2); plot(x2,y2,'ko', x2,y2,'r-');  
xlabel('desired width');  
ylabel('actual width');  
title('chip 2');
```

The second chip is considered as a good one. The actually width of the wire is very close to the desired width. Thus the data generates a reasonable well linear plot.

Data for the third plot

Actual Width Y-axis (μm)	Programmed Width Y-axis(μm)
46.9941	50
19.0768	20
6.0487	10

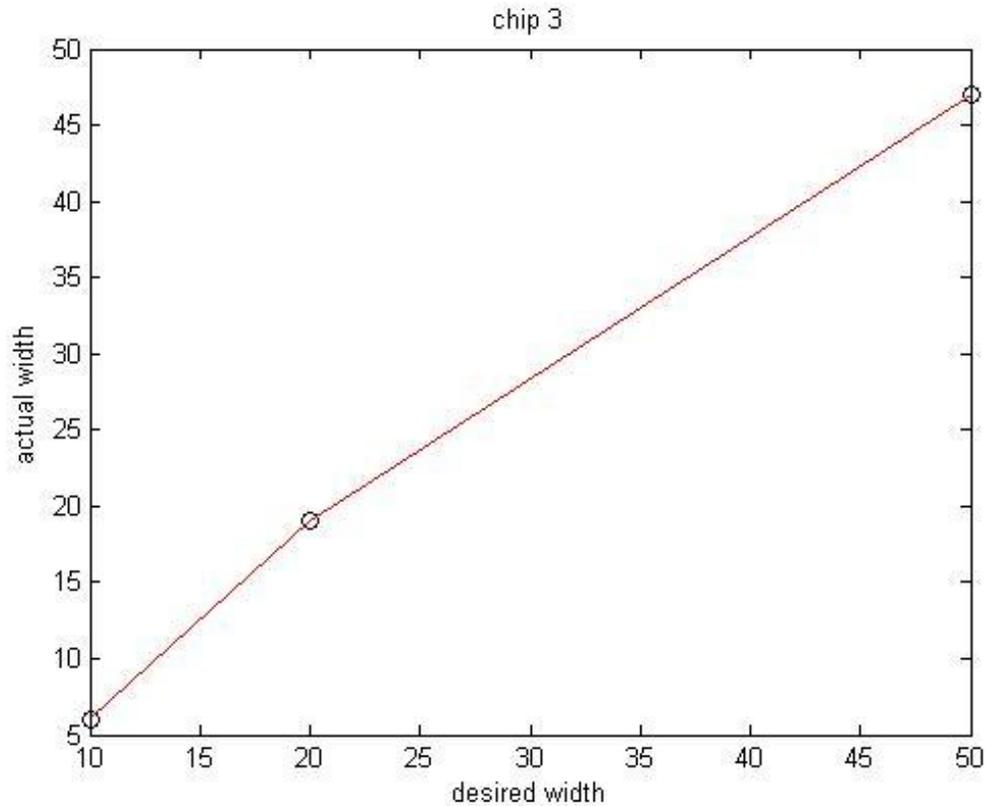


Figure 4

The matlab code to generate this plot is shown below:

```
x3=[50,20,10];  
y3=[46.9941,19.0768,6.0487];  
figure(3); plot(x3,y3,'ko', x3,y3,'r-');  
xlabel('desired width');  
ylabel('actual width');  
title('chip 3');
```

The third chip has a bad data point (10, 6.0487). This wire was ablated by the laser back and forth several times. Therefore, the wire is too narrow from the desired width. Also, since the laser has run over the gold several times, the substrate has been damaged and thus results the dark area shown in figure 1.

Since the data for the second and third chip shows a linear relationship except the last data from chip 3, the data from chip 2 and the first 2 data from chip 3 are combined together for the fourth graph to further investigate the linear behavior of the width of the wire.

Actual Width Y-axis(μm)	Programmed Width X-axis (μm)
46.994	50
93.0576	100
192.9084	200
46.9941	50
19.0768	20

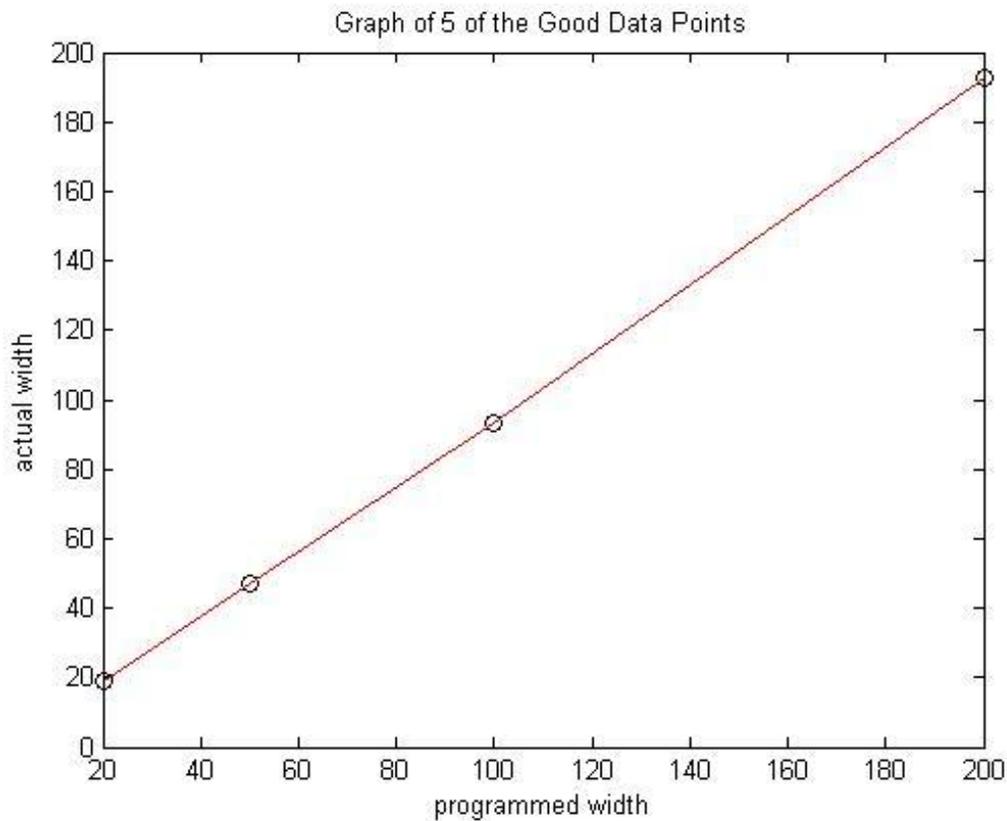


Figure 5

The matlab code to generate this plot is shown below:

```
x4=[20,50,50,100,200];
y4=[19.0768, 46.9941, 46.994,93.0576,192.9084];
plot(x2,y2,'ko',x2,y2,'r-');
xlabel('programmed width');
ylabel('actual width');
title('Graph of 5 of the Good Data Points');
```

As shown by the graph, the plot is roughly linear.

The data points are fitted with Matlab using linear fitting option.

This graph is fitted from the data of the first plot

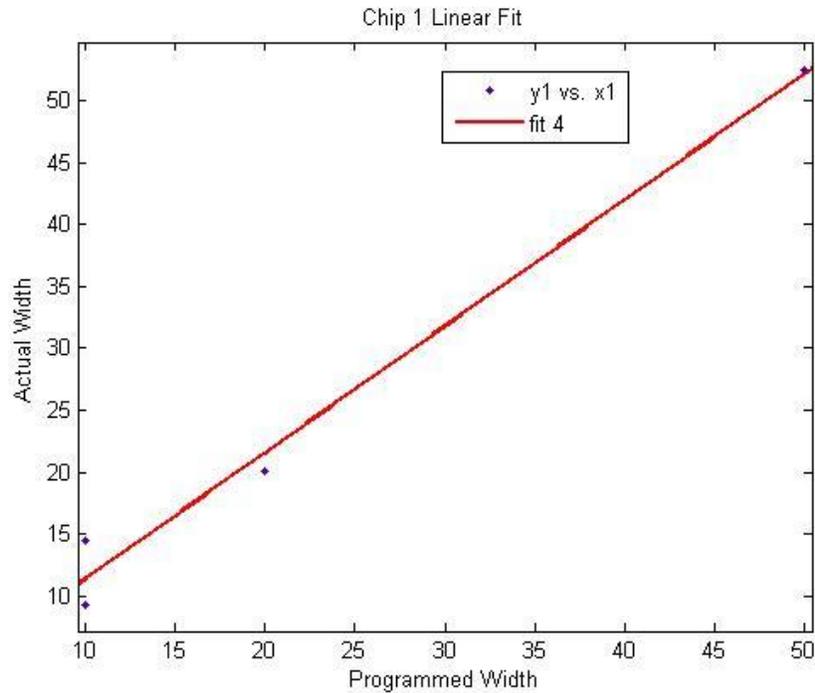


Figure 6

Linear model Poly1:

$$f(x) = p1*x + p2$$

Coefficients (with 95% confidence bounds):

$$p1 = 1.023 (0.6493, 1.396)$$

$$p2 = 1.071 (-9.32, 11.46)$$

Goodness of fit:

SSE: 16.18

R-square: 0.9858

Adjusted R-square: 0.9787

RMSE: 2.844

The slope of the linear fit is greater than 1 because of the data point (10, 14.4239). Since the actual width is far greater than the programmed width, the slope of the overall fitting is increased above 1.

This graph is fitted from the data of the second plot

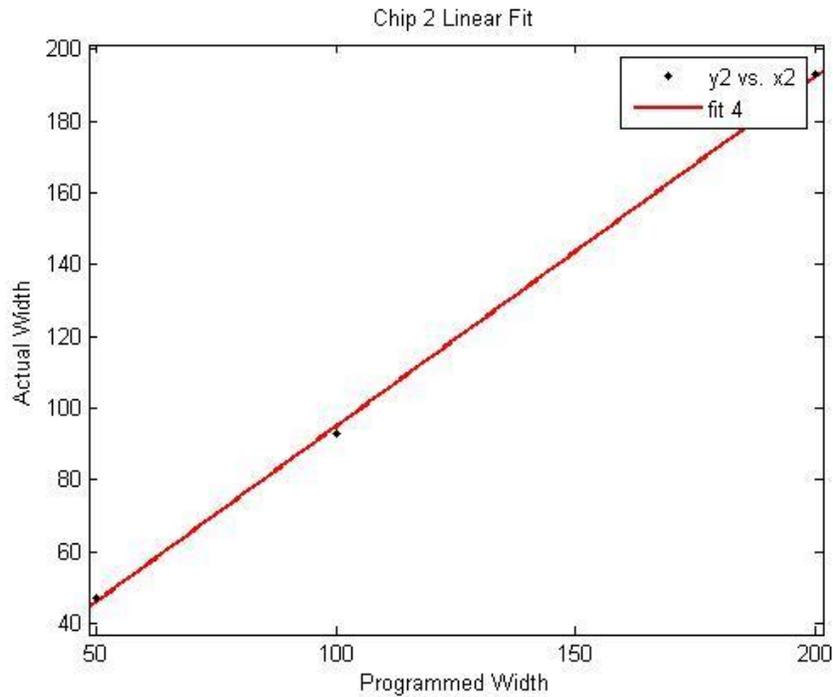


Figure 7

Linear model Poly1:

$$f(x) = p1*x + p2$$

Coefficients (with 95% confidence bounds):

$$p1 = 0.9764 (0.7336, 1.219)$$

$$p2 = -2.931 (-35.05, 29.19)$$

Goodness of fit:

SSE: 4.261

R-square: 0.9996

Adjusted R-square: 0.9992

RMSE: 2.064

This graph is roughly linear and the slope is less than 1 which means the actual width is smaller than the programmed width. The intercept means the backlash of the machine.

This graph is fitted from the data of the third plot

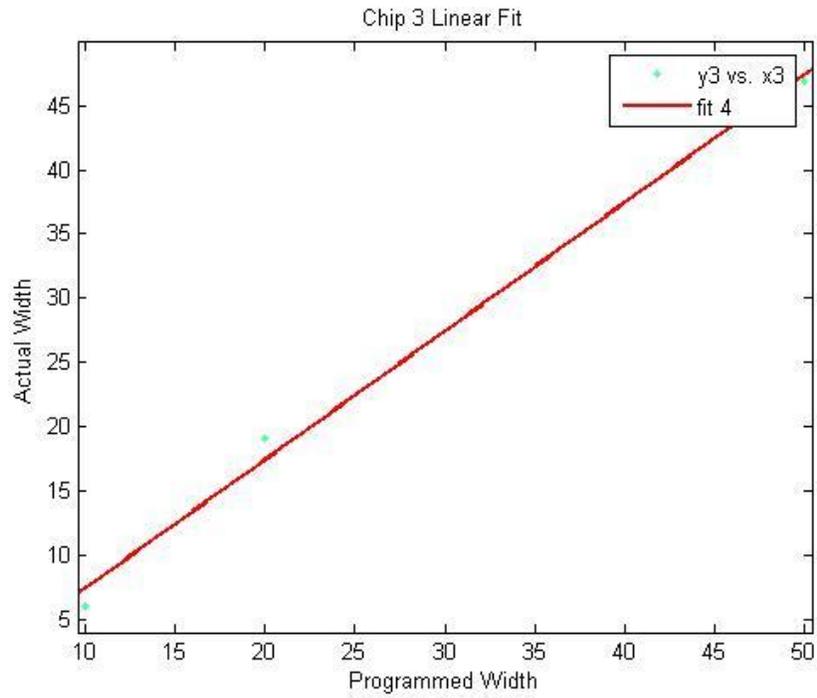


Figure 8

Linear model Poly1:

$$f(x) = p1*x + p2$$

Coefficients (with 95% confidence bounds):

$$p1 = 1.002 (0.05693, 1.947)$$

$$p2 = -2.684 (-32.58, 27.21)$$

Goodness of fit:

SSE: 4.796

R-square: 0.9945

Adjusted R-square: 0.989

RMSE: 2.19

H. Previous SEM Data and Analysis

The following is a report that was previously submitted to the project sponsors for review.

The image is collected by the secondary detector and therefore, the result of analysis is incomparable with the result from the primary detector. However, this will give the reader an qualitative idea of the wire characterization.

Currently, there are three prototype atom chips fabricated. The chip being analyzed in this report is the chip with four sets of wires: a 20 μm wire, a 50 μm wire and a set of two 10 μm wires. This chip is also known as the “Bad” chip because of the double 10 μm wire that are closely intertwined and the numerous scratches on the gold surface of the chip.

The surface image of the chip was taken by an SEM from EOS and the image of the 20 μm wire is shown below. A rough estimation of the width of the picture shows 80 μm . Since the wire is 20 μm wide, a line drawn connecting the left and right edge of the gold wire would be 20 μm wide. This line is shifted to start from the right edge of the image and is copied and pasted to increase the length of the wire until it reaches the left edge of the graph. The wire was arrayed four times until it barely reaches the left edge of the image. Therefore, the graph is estimated to be 80 μm with a ± 5 μm error of estimation. Since, there are a total of 2576 pixel columns spanning in the x-direction and 1936 pixel columns spanning in the y-direction, each pixel is estimated to be:

$$80 \mu\text{m} / 2576 = 0.0310559 \mu\text{m}$$

This number will be used in the calculation of the mean and variance of the edge of the cuts.

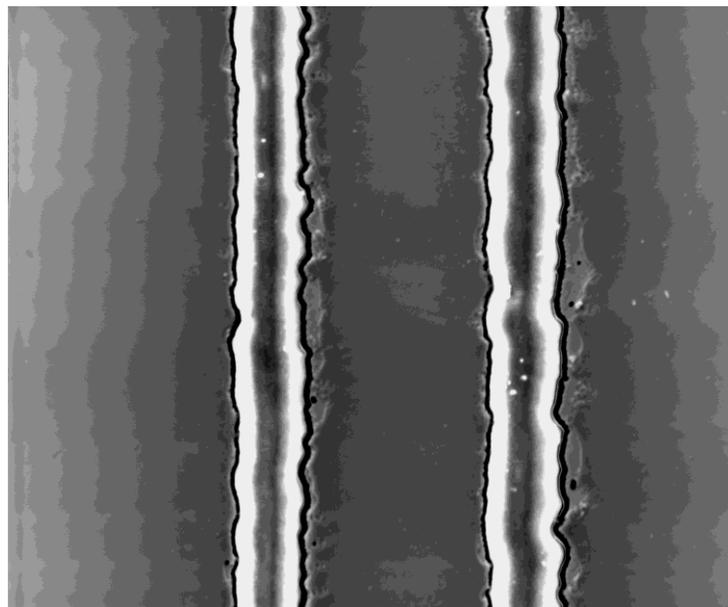


Figure 1: SEM Image of the 20 μm wide wire

The image is divided into smaller portions featuring the wire ablation edges for analysis. The analysis is done with Matlab. First, the x-direction pixels are separated into regions by inspecting columns of the image. The separation process is carried out by the following lines of code:

```
image = rgb2gray(imread('20UM.jpg')); % load the image and convert into a matrix of numbers.  
imshow(image(1: 1936,LBOUND:RBOUND)); % show the image column and adjust the pixels.
```

image1 = image(1:1936,LBOUND:RBOUND); % transfer part of image into image1.
 Repeat the above process by observing the graph until the data to be analyzed is picked out. The following four portions were picked out featuring the ablation edges.



a) 1st left edge b) 1st right edge c) 2nd left edge d) 2nd right edge

Figure 2: Wire Ablation Edge Portions

Using the code attached in appendix and the isolated data shown above, the mean and the variance of the edge of the cut is estimated below. The units are all in micrometers (μm). The mean values starts from the left edge of the graph.

	20 μm 1 st L-Edge	20 μm 1 st R-Edge	20 μm 2 nd L-Edge	20 μm 2 nd R- Edge
Mean	24.988	32.796	53.293	61.042
Variance	0.048871	0.11854	0.11854	0.088058

The following graph is generated by analyzing the 1st left edge on the chip. The data is obtained from the original intensity matrix by the following command:

```
image1 = image(1:1936,750:850);
[u, v] = processr(image1, 750);
```

The data set generated from the above command is an intensity matrix that has 101 columns and 1936 rows. Each element is a value from [0, 255]. 255 represents pure white while 0 represents pure dark. The values in between has intermediate brightness. The code will detect the minimum value of each row and then plot it against the number of rows.

By analyzing the first set of data with the Matlab program, the original edge of the cut and the estimated edge of the cut is shown in the figures below. The left image is the original one. The image ignores all the intensity values from [70, 255]. Then, the right graph is generated from the analyzed data by plotting it as an image. The two patterns roughly match with each other which means the analysis is reasonably accurate.

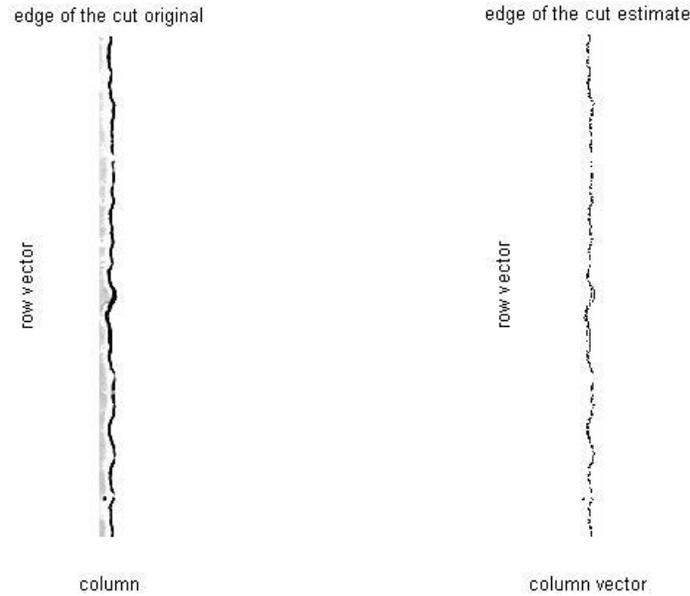


Figure 3: Edge Comparison of 1st Left Edge

The following graph is generated by plotting the pixel of the minimum intensity value in each row against the row value. The graph roughly reproduces the shape of the edge of a cut. According to the graph, the y-axis data are generally accumulated within the range of [40, 70]. The mean value is roughly 55 pixels away from 0, and varies by ± 15 pixels around the mean. As one may have noticed that there are actually 4 bad data points that are far below the actual mean value. This may result in a lower mean value and a larger standard deviation value.

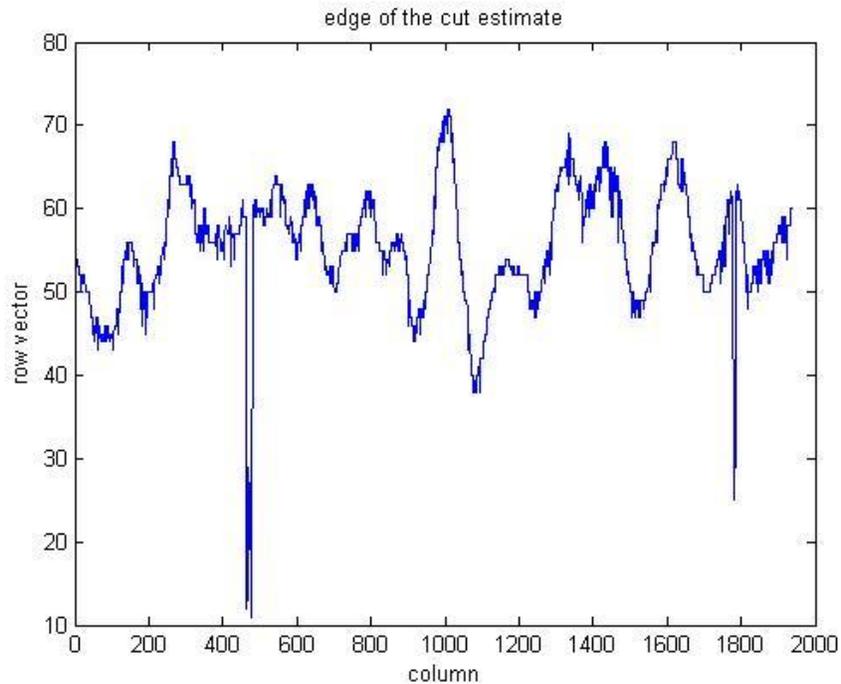


Figure 4: pixel of the minimum intensity value in each row against the row value

The following graph is generated by analyzing the 1st cut right edge on the chip. The data is obtained from the original matrix by the following command:

```
image2 = image(1:1936,990:1100);
[u, v] = process(image2, 990);
```

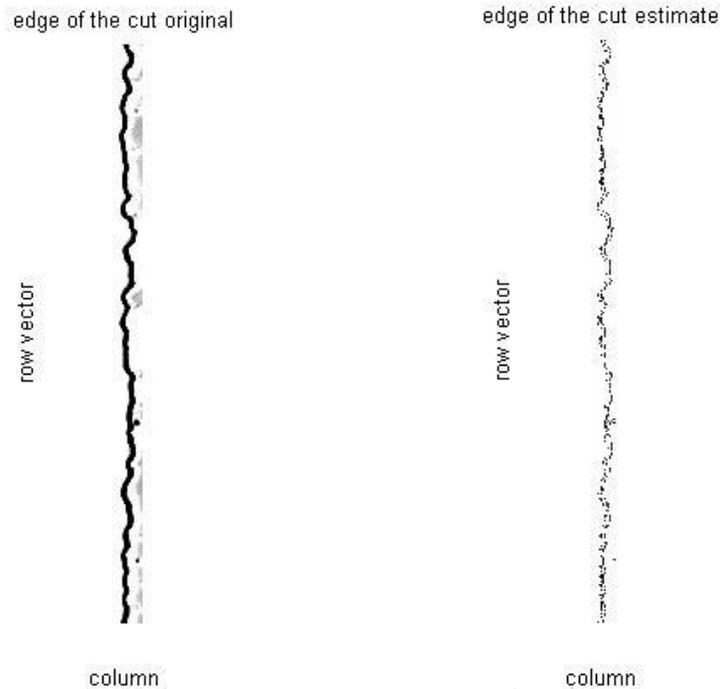


Figure 5: Edge Comparison of 2nd Left Edge

The left one is the original right cut intensity graph plotted by omitting the intensity data that are outside the range of [0, 80]. The right graph is fitted from the minimum values that were extrapolated from the intensity matrix. The pattern of the two cuts roughly matches which means that the estimation is reasonable.

However, the following graph demonstrates a high variation of the pixel of minimum intensity value. Although the values mostly stay in the range of 45 to 85, there are quite a few points that are in the range from 85 to 100. This result might be owing to the Matlab program that analyzes the data. The program first determines the minimum intensity values in each row. Then find the minimum intensity value in each row. If there are several values that stay at minimum, the pixel of the last value is picked. If there is only one minimum, the pixel of that minimum value is picked. The data points that are in the range of [85, 100] might be because the minimum intensity values aren't generated near the area of a cut but at some other areas far away. Such data can be omitted if the Matlab program introduces a logic structure that could force the minimum values to be within the range of a cut.

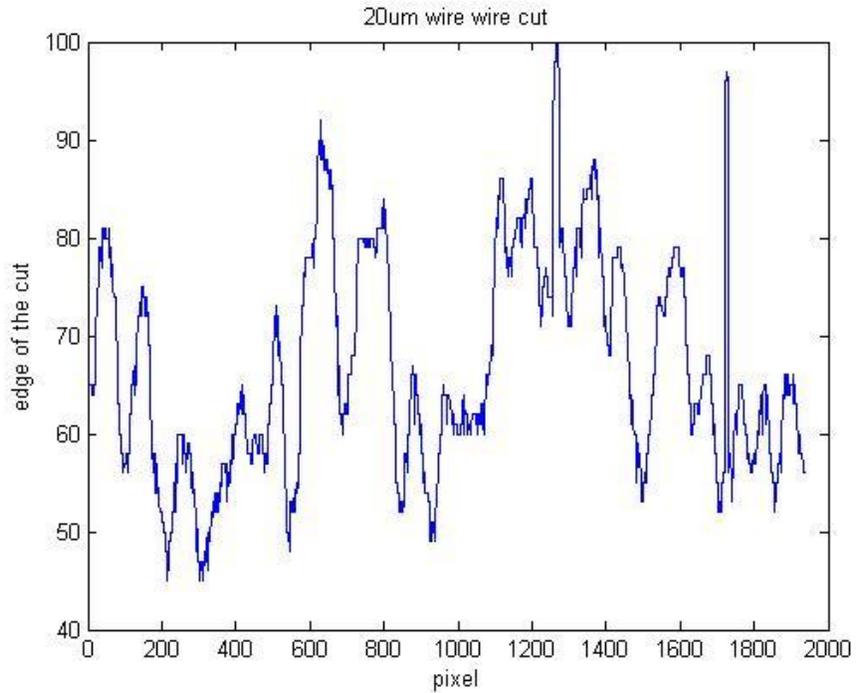


Figure 6: pixel of the minimum intensity value in each row against the row value

The following graph is generated by analyzing the 2nd cut right edge on the chip. The data is obtained from the original matrix by the following command:

```
image3 = image(1:1936,1650:1750);
[u, v] = processr(image3, 1650);
```

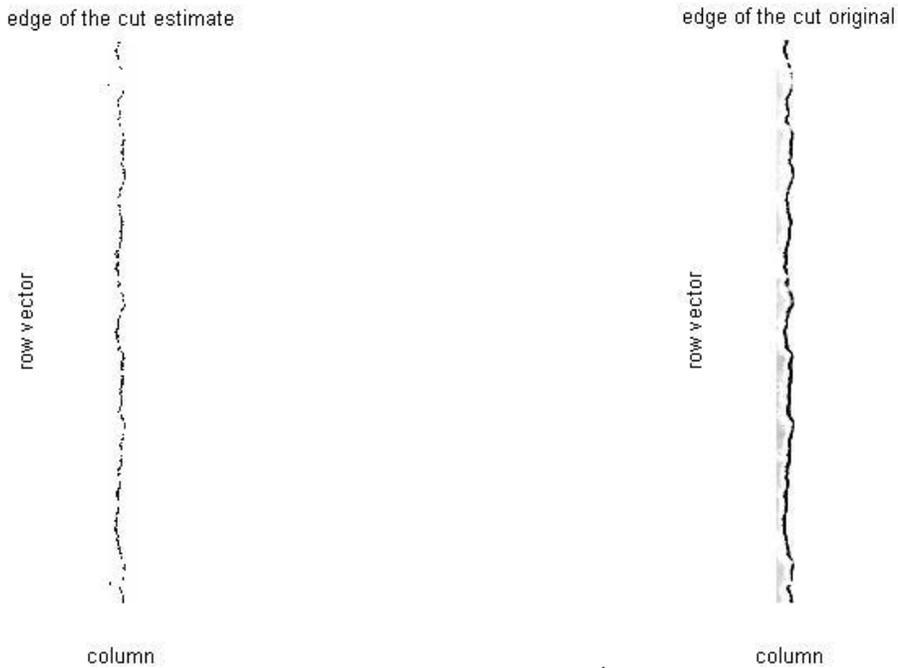


Figure 7: Edge Comparison of 3rd Left Edge

The lighter graph on the left is the estimated graph from the extrapolated minimum intensity values. The graph on the right is the original graph plotted by omitting the intensity data in the range of [70, 255]. The two graphs demonstrate similar patterns except a few dark dots that are away from the main path. This feature is clearly reflected in the following graph.

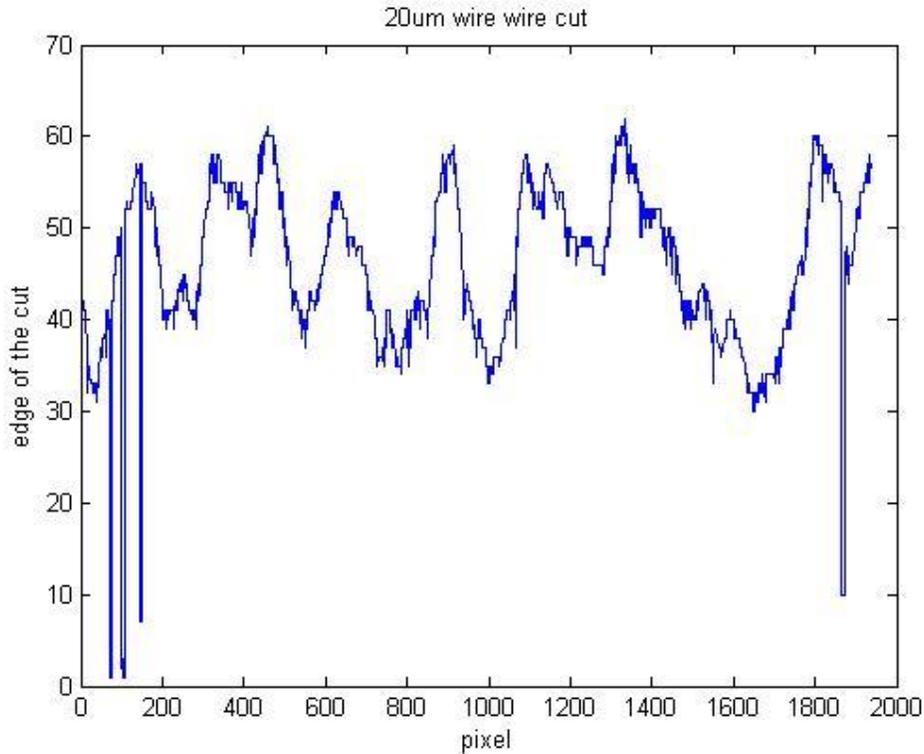


Figure 8: pixel of the minimum intensity value in each row against the row value

The graph above shows a reasonably well pattern. The y-direction values of are roughly in the range of [30, 60]. The average is around 45 pixels. The value varies in a range of ± 15 pixels. This agrees with the mean calculated above and shows that the variance for the left cut is smaller than the right cut which also agrees with the calculated value in the table above. There are also 5 bad data points that are in the range of [0, 10] pixels. The bad data points could potentially decrease the mean and increase the variance.

The following graph is generated by analyzing the 2nd Right Edge on the chip. The data is obtained from the original matrix by the following command:

```
image3 = image(1:1936,1650:1750);
[u, v] = processr(image3, 1650);
```

Two black and white graphs are generated below. The left one is the estimated pattern of the cut from the extrapolated data while the right one is the plot of the actual data by ignoring intensity values outside the range of [0, 80]. The two graphs show similar edges of cuts. There are a few isolated dark dots that are off from the main path. These dots represent the minimum intensity value in a row and would result a rather discontinuous graph of minimum-intensity-row-pixel vs. row-pixel.

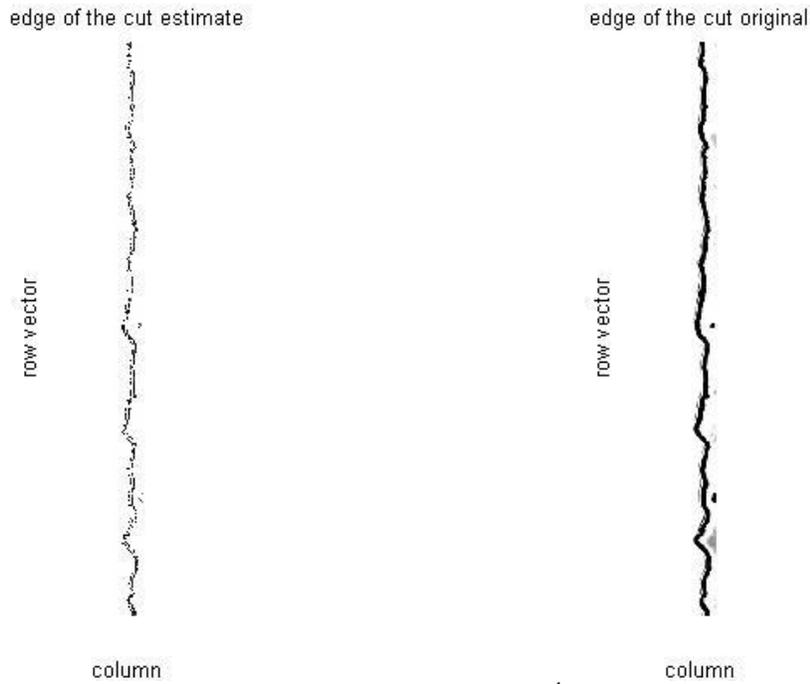


Figure 9: Edge Comparison of 4th Left Edge

The following graph has minimum intensity pixels in the range of [40, 80] with a few bad data points in the range of [90, 100]. These bad data points cause discontinuity in the path of the cut, and will increase the value for the mean and the variance.

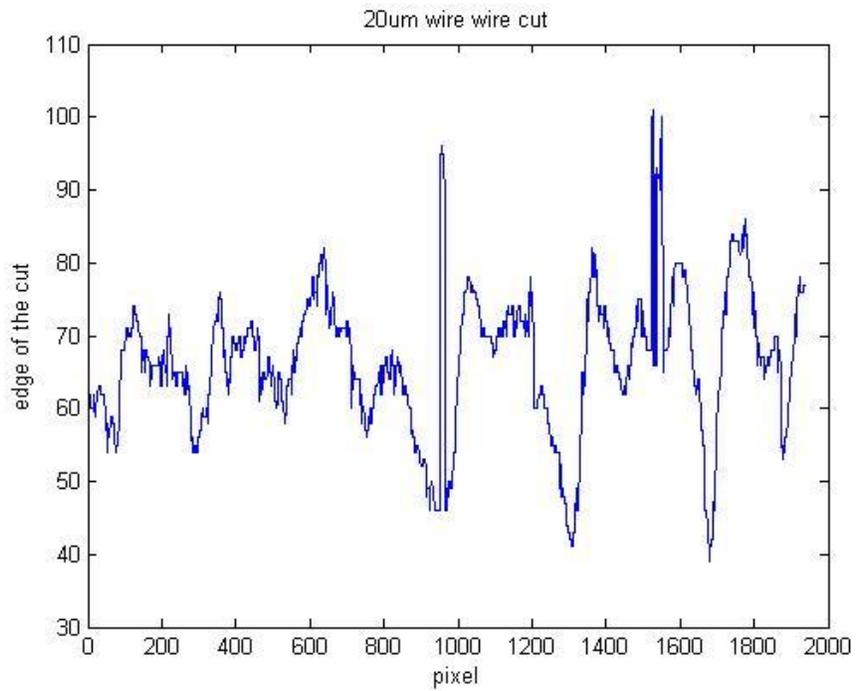


Figure 10: pixel of the minimum intensity value in each row against the row value

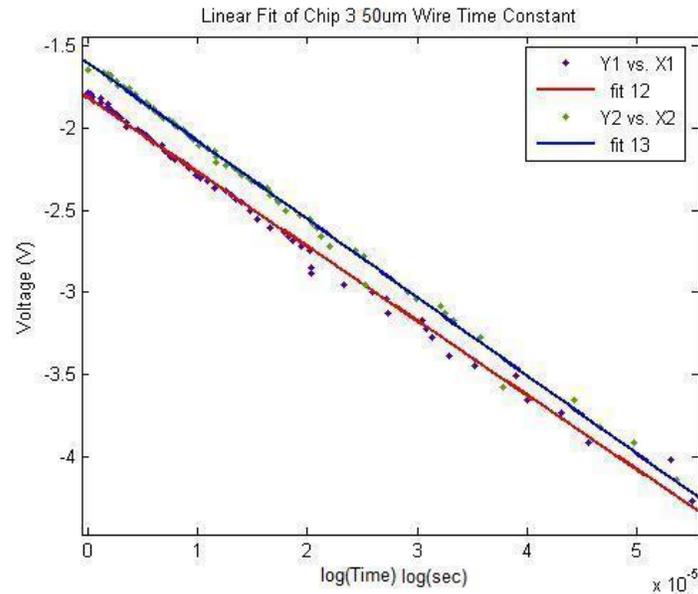
I. Wire Resistance Data

Some of the 2 point contact resistance measured with the digital multimeter is listed here. The resistance was measured at the beginning of the testing and at the end. Some wires' resistances are listed as N/A because either a connection could not be established.

	2 Point Resistances (Ω)		
Wire	Before	After	Tested with Constant Current?
Chip 2 200 μm wire	15.2	37.4	Yes
Chip 2 100 μm wire	28	67.1	Yes
Chip 2 50 μm wire	N/A	N/A	No
Chip 3 50 μm wire	50.95	51.16	No
Chip 3 20 μm wire	114.35	114.3	No
Chip 3 10 μm wire	315.3	315.3	No

J. IV Data

Additional result of fitting for the data from the 50um wire is provided below. The method of analysis is the same as the method above. And the fitted time constant is substituted into the fitting equation for the charging part of data to check it quantitatively



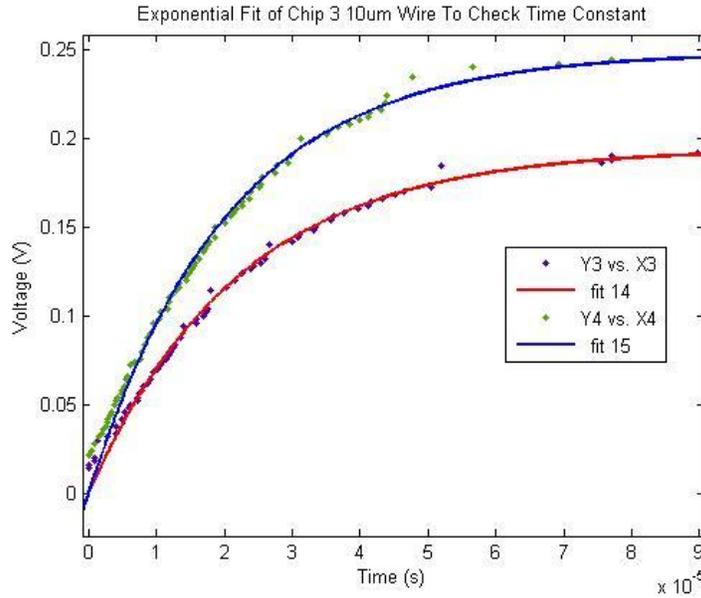
Fitting of the Voltage Response of the Falling Part of the Edited Data Time 100ms

Linear model Poly1: (fit 12 Pulse Width 500us)	Goodness of fit:
$f(x) = p1*x + p2$	SSE: 0.124
Coefficients (with 95% confidence bounds):	R-square: 0.9948
p1 = -4.524e+004 (-4.609e+004, -4.438e+004)	Adjusted R-square: 0.9947
p2 = -1.819 (-1.837, -1.802)	RMSE: 0.04584

Fitting of the Voltage Response of the Falling Part of the Edited Data Time 100us

Linear model Poly1: (fit13 Pulse Width 500ms)	Goodness of fit:
$f(x) = p1*x + p2$	SSE: 0.08338
Coefficients (with 95% confidence bounds):	R-square: 0.9965
p1 = -4.759e+004 (-4.828e+004, -4.69e+004)	Adjusted R-square: 0.9965
p2 = -1.607 (-1.62, -1.593)	RMSE: 0.03528

Result of the fitting for the charging part of the data.



General model: (fit14 Pulse Width 500us)	Goodness of fit:
$f(x) = a*(1-\exp(-b*x))$	SSE: 0.001448
Coefficients (with 95% confidence bounds):	R-square: 0.9915
a = 0.1942 (0.1896, 0.1987)	Adjusted R-square: 0.9914
b = 4.481e+004 (4.26e+004, 4.703e+004)	RMSE: 0.004832

General model: (fit15 Pulse Width 500ms)	Goodness of fit:
$f(x) = a*(1-\exp(-b*x))$	SSE: 0.00295
Coefficients (with 95% confidence bounds):	R-square: 0.9905
a = 0.2483 (0.2421, 0.2545)	Adjusted R-square: 0.9904
b = 4.868e+004 (4.625e+004, 5.111e+004)	RMSE: 0.00619

The time constant is calculated with the equation 9 and 10 provided in section 5.4.

K. Contact Information

K.1 Report Authors

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K.2 Project Sponsors

Quantum Degenerate Gases Laboratory

The QDG Lab is a group at the University of British Columbia, in the research field of Atomic Molecular and Optical Physics (AMO).

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Dr. Bruce G. Klappauf is a research associate at the University of British Columbia, with research interests in Condensed Matter and AMO. klappauf@phas.ubc.ca

K.3 External Contacts

Earth and Ocean Science Electron Microbeam / X-Ray Diffraction Facility

The two contacts are Dr. Mati Raudsepp (mraudsepp@eos.ubc.ca) and Sasha Wilson (swilson@eos.ubc.ca). Use of the SEM is available at a rate of \$20 per hour.

<http://www.eos.ubc.ca/research/infrastructure/emxdf.html>

Microsystems and Nanotechnology Research Group

The Mina lab is located at Kaiser 4060. The two contacts are the director, Dr. Lukas Chrostowski (lukasc@ece.ubc.ca) and a visiting Post-Doc, Mark Greenberg (blackbyk@yahoo.com).

<http://www.mina.ubc.ca/kaiser4060>

AMPEL Nanofabrication Facility

The two contacts are Dr. Mario Beaudoin (beaudoin@physics.ubc.ca) and Dr. Alina Kulpa (alina@phas.ubc.ca). Use of the Profilometer is available for a fee with clean room training.

<http://www.ampel.ubc.ca/nanofab/>

Microelectromechanical Systems Laboratory

The contact is Dr. Boris Stoeber (Stoeber@mech.ubc.ca). Use of the Wyko white light interferometer is available at a rate of \$ 30 per hour. Equipment signup requires going to Gmail calendar, and searching “mems equipment”.

L. LDC 500 Specification Sheet



LASER DIODE CONTROLLERS

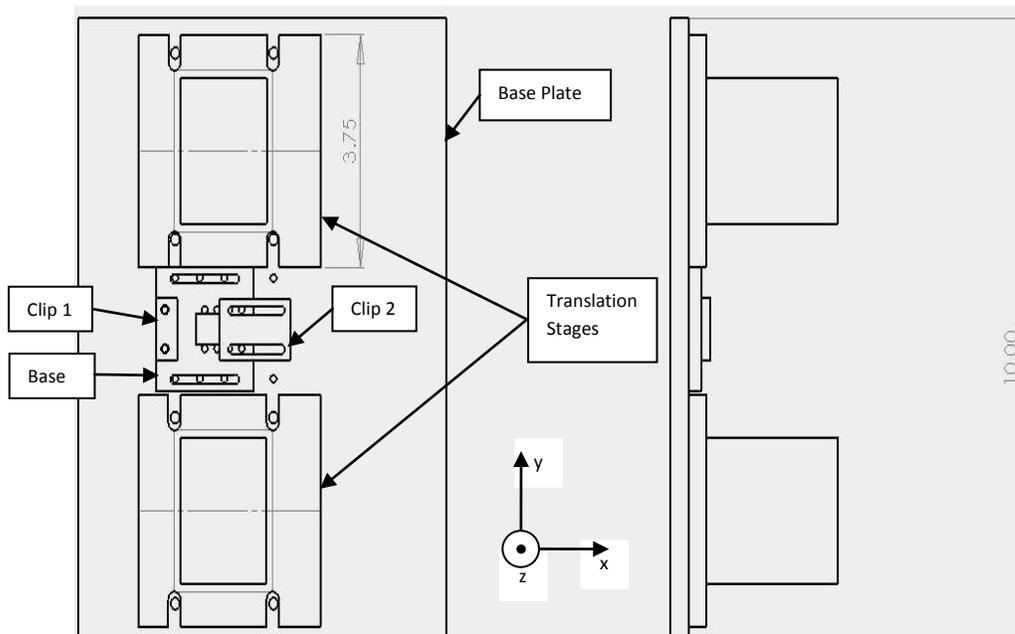
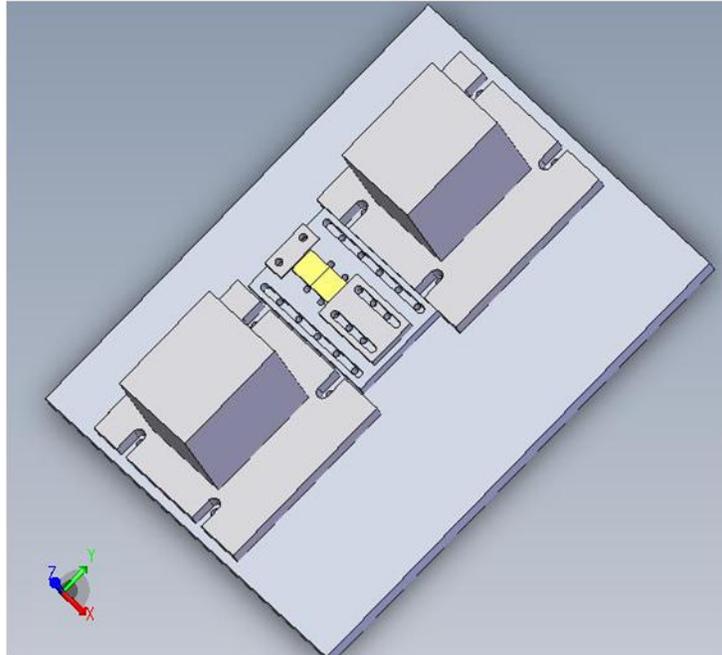
	LDC500	LDC2000	LDC201ULN	LDC202	LDC210	LDC220
Current Control						
Control Range (continuous)	0 to ± 500 mA	0 to ± 2 A	0 to ± 100 mA	0 to ± 200 mA	0 to ± 1 A	0 to ± 2 A
Compliance Voltage	>4	>4	>2.5 V	>6 V	>4 V	>4 V
Resolution	<5 μ A	<5 μ A	10 μ A	10 μ A	100 μ A	100 μ A
Accuracy	100 μ A	100 μ A	± 50 μ A	± 100 μ A	± 1 mA	± 2 mA
Noise(10 Hz to 10 MHz, RMS)	<2 μ A	<20 μ A	<0.2 μ A	<1.5 μ A	<5 μ A	<15 μ A
Ripple (50 Hz, RMS), typical	<2 μ A	<5 μ A	<0.5 μ A	<1.5 μ A	<3 μ A	<5 μ A
Transients, typical	<0.5 μ A	<2 mA	<50 μ A	<0.2 mA	<1 mA	<2 mA
Drift (30 min, 0 to 10 Hz), typical	<50 μ A	<200 μ A	<10 μ A	<20 μ A	<100 μ A	<200 μ A
Temperature Coefficient	<50 ppm/ $^{\circ}$ C	<50 ppm/ $^{\circ}$ C	<50 ppm/ $^{\circ}$ C	<50 ppm/ $^{\circ}$ C	<50 ppm/ $^{\circ}$ C	<50 ppm/ $^{\circ}$ C
Power Control						
Control Range Photo Current	5 μ A to 2 mA					
Resolution Photo Current					0.1 μ A	
Accuracy	0.1 μ A	0.1 μ A			± 2 μ A	
Current Limit						
Setting Range			0 to ≈ 100 mA	0 to ≈ 200 mA	0 to ≈ 1 A	0 to ≈ 2 A
Resolution	100 μ A	100 μ A	10 μ A	10 μ A	100 μ A	100 μ A
Accuracy	± 1.5 mA	± 5 mA	± 0.5 mA	± 0.5 mA	± 2.5 mA	± 5 mA
Modulation, Analog Control Input						
Input Resistance	10 k Ω					
Modulation Coefficient, CC	50 mA/V	200 mA/V	10 mA/V $\pm 5\%$	20 mA/V $\pm 5\%$	100 mA/V $\pm 5\%$	200 mA/V $\pm 5\%$
3 dB Bandwidth DC	150 kHz DC	50 kHz DC	3 kHz DC	250 kHz DC	100 kHz DC	50 kHz
Modulation Coefficient, CP	0.2 mA/V $\pm 5\%$					
Control Output for Laser Current						
Load Resistance					>10 k	
Transmission Coefficient			100 V/A $\pm 5\%$	50 V/A $\pm 5\%$	10 V/A $\pm 5\%$	5 V/A $\pm 5\%$
Connectors						
Laser Diode, Photodiode, LASER ON signal, Interlock	DB9 Female	DB9 Female	9-pin D-sub			
Modulation Input	BNC					
Control Output Laser Current	BNC					
Chassis Ground	4 mm banana					
General Data						
Line Voltage	110 V $\pm 10\%$, 115 V $\pm 10\%$, 230 V $\pm 10\%$					
Line Frequency	50 to 60 Hz					
Maximum Power Consumption	30 W	60 W	13 W	15 W	30 W	45 W
Operating Temperature	0 to +40 $^{\circ}$ C					
Storage Temperature	-40 $^{\circ}$ C to +70 $^{\circ}$ C					
Warm-up Time for Rated Accuracy	10 min					
Weight	<6.6 lb.			<3 kg		
Dimensions (W x H x D)*2	5.8 x 2.8 x 12.5"			146 x 66 x 290 mm		

M. IV Test Bench CAD Drawings

Note:

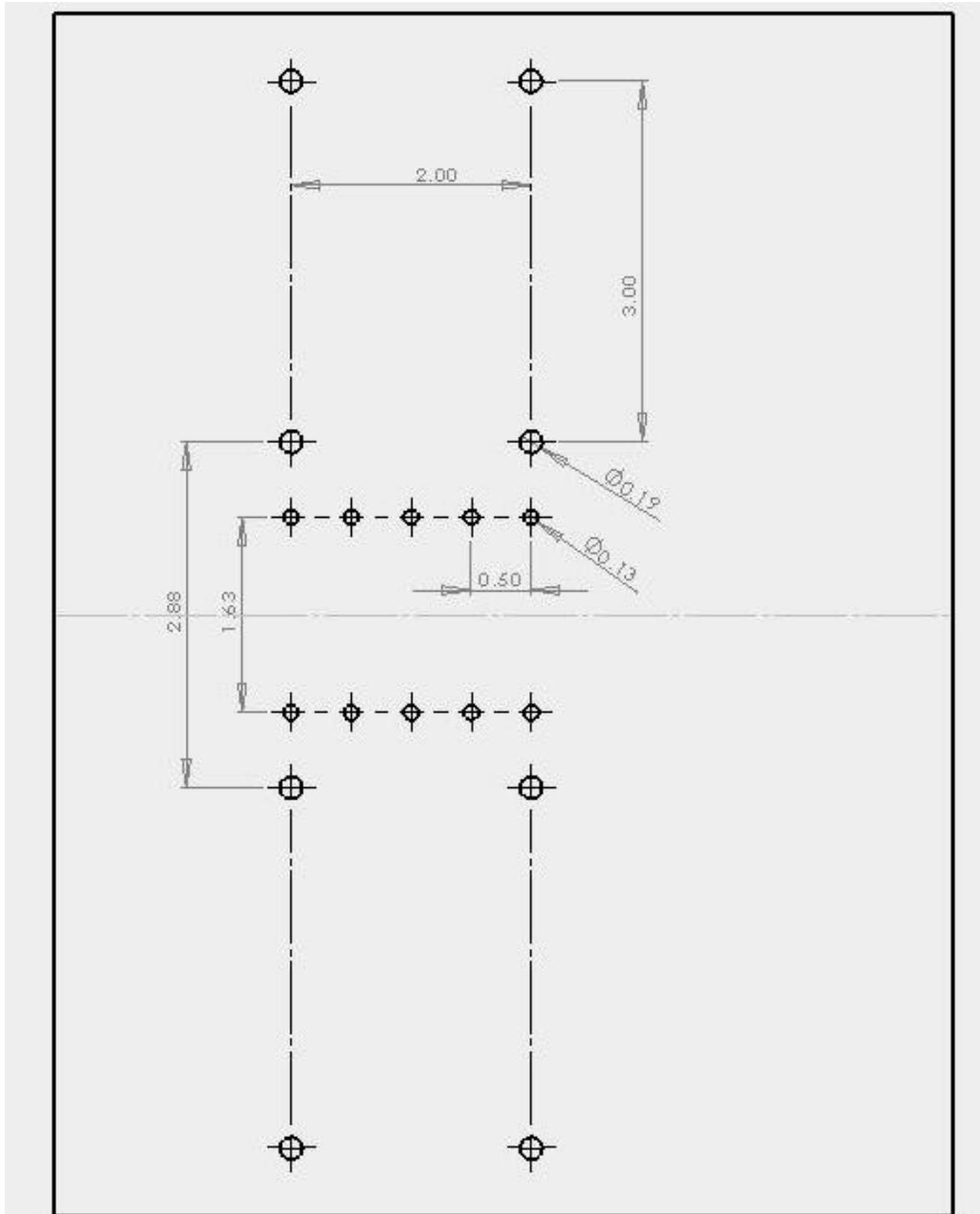
- All Dimensions are in Inches.
- Drawings are not to scale

Test Bench arrangement

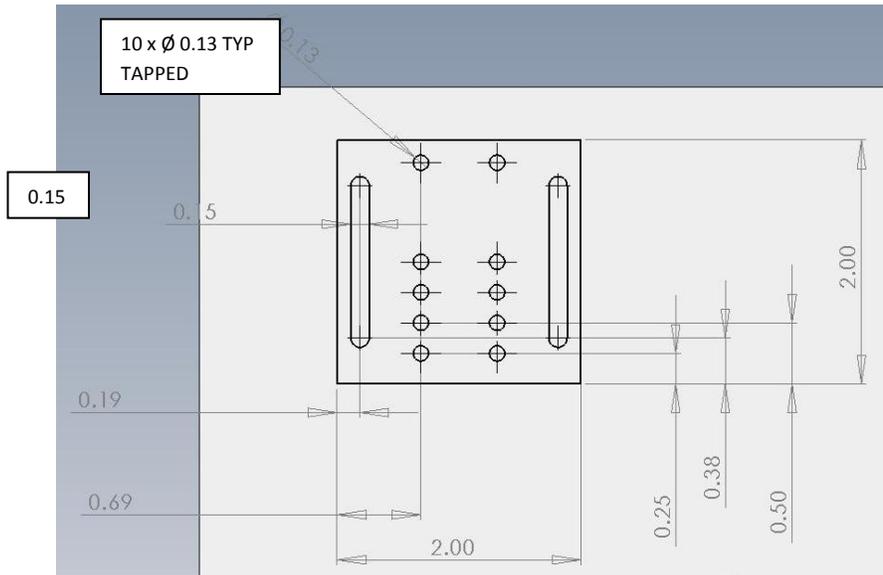


Base Plate

The base plate is where the translation stages and the chip holder are held in place. This is designed for the purpose of carrying the test bench assembly. The following Drawing shows the hole patterns that are drilled. The base plate size that was used is 10" x 8" x 3/8". All Holes need to be tapped.

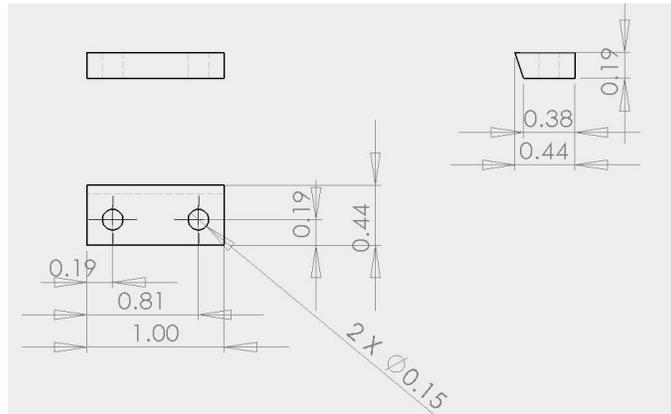


Base



Clip 1

The slant can be made with a file. The Holes are not tapped.



Clip 2

